A Simple PWM scheme for a four-level dual-inverter fed open-end winding five-phase motor drive

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Abstract

A simple PWM scheme for a four-level dual-inverter fed open-end winding (OeW) five-phase motor drive is discussed in this paper. The proposed PWM scheme adapts the decomposition PWM scheme of dual-inverter fed five-phase drive with equal DC-link voltage. The modulation strategy operates at three different modes according to modulation index (M). When modulation index, $M > 0.35$, inverter 1 operates at fundamental frequency while inverter 2 operates in PWM mode. When $M \leq 0.35$ only inverter 2 operates in PWM mode while inverter 1 is locked at zero switching state (11111 or 00000). The proposed PWM schemes is verified using Matlab/simulink. The results show that the quality of the output voltages improves in comparison with the voltage output of three-level inverter for all modulation indices. The inverter performance is also improved compared to the previous four-level PWM scheme (URS PWM) especialy for $M > 0.35$ while for $M \leq 0.35$, the performance is exactly the same as the four-level URS PWM scheme. One drawback of the proposed PWM scheme is that an additional circuit is required to reduce the DC-link voltage of inverter 1 at the particular speed ranges of $0.35 < M \leq 0.7$.

1. Introduction

Multi-level inverters have been intensively studied over decades with particular objectives to improve the converter performance as well as to increase the power rating of inverter hence it is suitable for medium-high power application drives. Various topology of multi-level inverter (MLI) has been developed, include the neutral point clamped (NPC), the flying capacitor (FC) and the cascaded converters [1, 2, 3]. Lately, a dual-inverter fed open-end winding (OeW) configuration was intruduced in 1993 by Stemmler and Guggenbach. In the OeW structure, the neutral point of machine is open, allowing the machine is fed from both end using two inverters [4].

Space vector PWM (SVPWM) schemes for the dual-inverter fed OeW three-phase motor drives have been masively investigated in the last two decades. Most of the schemes are developed for improving the output voltage quality, reducing the converters losses and development of simpler modulation strategies [5,6]. The structure may consist of two two-level inverters or combination of multi-level and two-level inverter with various ratio of DC-link voltage [7,8]. However, in conjunction with multi-phase machine drives, development of PWM schemes for dual-inverter fed structure presents a considerable challenge due to the existency of huge number of voltage vectors which are mapped in multiple two-dimentional planes. In addition, the behavior of multi-phase machine is different as the three-phase machine. In a five-phase machine with nearly sinusoidal magneto-motive force, only harmonics components mapped in α-β plane are able to develop useful torque, while the harmonics mapped in x-y plane relate to the motor losses (copper losses and friction losses). The development of a PWM strategy must therefore simultaneously consider both 2D subspaces [9]. This fact further increase the complexity in the development of PWM scheme and the available PWM schemes for three-phase drives cannot directly be applied for five-phase machine drives

Fig. 1 shows the simplified diagram of dual-inverter fed OeW five-phase motor drives. Two-level five-phase inverter can generate $5^2 = 32$ voltage space vectors in two two-dimensional planes as shown in Fig. 2. In the dual-inverter fed structure, when two two-level five-phase inverter are applied, combination of the 32 x 32 switching states results in 1024 switching states. The number of voltage space vectors depends on the ratio of DC-link voltage. When equal ratio of DC-link voltage is applied, the 1024 switching states mapped in 211 space vector locations [10]. While when ratio DC-link voltage of 2: 1 is applied, this structure produces 781 voltage space vectors in both α-β and x-y planes. Distribution of the voltage space vectors in α-β plane for both equal and DC-link ratio of 2:1 are shown in Fig. 3 and Fig 4 respectively. Distribution of voltage space vectors in the x-y planes are the same as in the α-β plane hence they are not shown.

It is shown from Fig. 3 and Fig. 4 that the distribution of the voltage space vectors formed a three-level and a four-level voltage space vectors single-sided supply drive

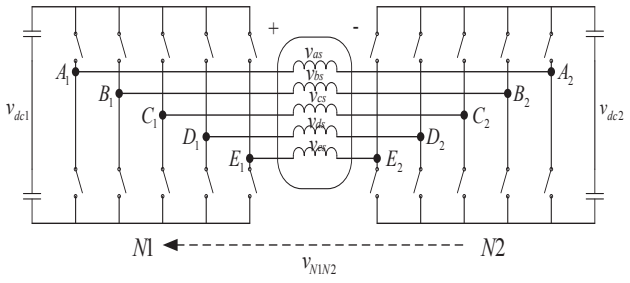
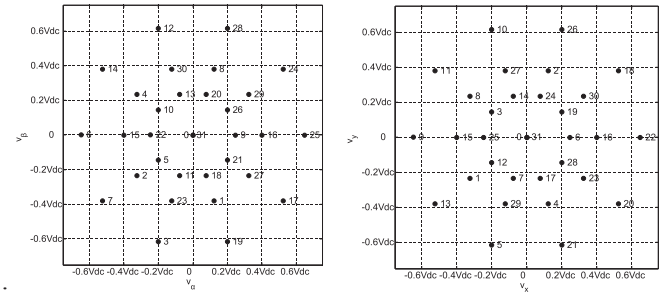


Fig. 1. The simplified topology of the dual two-level inverter fed a five-phase open-end winding motor drive.



(a) (b)

Fig. 2. Two-level five-phase VSI space vectors in the α-β and x-y planes.

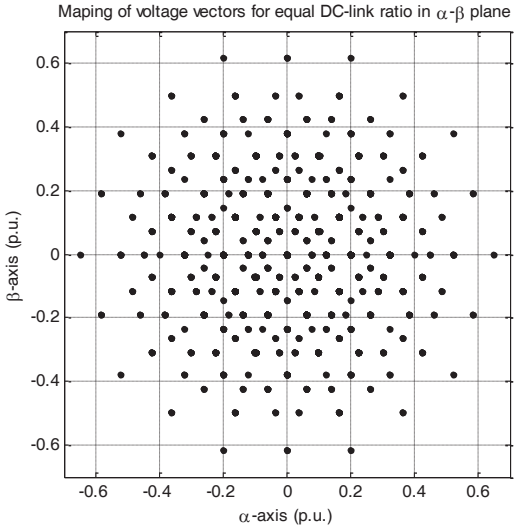


Fig. 3. Voltage space vectors distribution of a dual-inverter fed OeW 5-phase drive with equal DC-link voltage in the α-β plane.

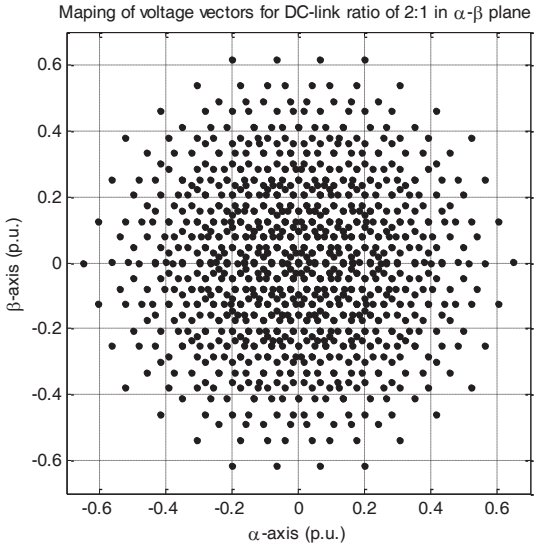


Fig. 4. Voltage space vectors distribution of a dual-inverter fed OeW 5-phase drive with DC-link voltage ratio of 2: 1 in the α-β plane.

equivalent for equal and ratio DC-link voltage of 2 : 1, respectively. When equal DC-link is applied, the voltage space vectors consist of highly redundant vectors (redundant vectors are the vectors that are formed by more than one switching states combination) while when ratio DC-link of 2: 1 is applied, the voltage vectors are distributed more spreadly.

As far as the SVPWM scheme in concern, the development of siutable PWM schemes for the dual-inverter fed OeW five-phase drives is considerably difficult. It is therefore the existing PWM schemes are developed by spliting the voltage references and then applying the carrier based PWM method for each inverter [11,12]. Furthermore, when un-equal DC-link voltage is applied, the possibility of the two inverters operate in unbalance condition increases as a result of the overcharged of capacitor DC-link voltage of one inverter. It is therefore hence an additional concideration must be taken in the development of PWM scheme.

This paper proposes a new PWM strategy of a four-level dual-inverter fed OeW five-phase drive. The developed PWM scheme adapts the decomposition PWM method [13-14] which operates one inverter at fundamental frequency and another inverter in PMW mode. The necessary adjustment is made to increase inverter performance. The proposed PWM scheme is verified using MATLAB and the performance is compared with the existing PWM methods. The proposed PWM method is explained detaily in Section 3

2 Existing PWM methods of four-level dual-fed OeW motor drive

Prior to discussing the proposed PWM scheme, the existing PWM methods for a four-level dual-inverter fed OeW five-phase motor drive are reviewed first. Until now only a few publications discuses PWM methods for a four-level dual-inverter fed OeW five-phase drive includes Darijevic et al (2013) and Jones et al (2014). Darijevic et al (2013) presents PWM methods based on carrier based (CB) PWM. According to distribution of the carriers, two types of level-shifted CB PWM (i.e PD and APOD CB PWM) were investigated. The modulation signals are generated by injecting the low-order harmonics using min-max method. Since in four-level inversion needs three carrier signals, a necesary modification is carried out. Switching states S_{ji}, are obtained using a simple mathematical equation (1) and the comparison of the voltage reference and the carrier signals are shown at Fig. 5 [11]

$$A_{ki} = \begin{cases} \text{if } v_i^* \geq C_k \text{ then } 1 \\ \text{if } v_i^* < C_k \text{ then } 0 \end{cases} \qquad (1)$$

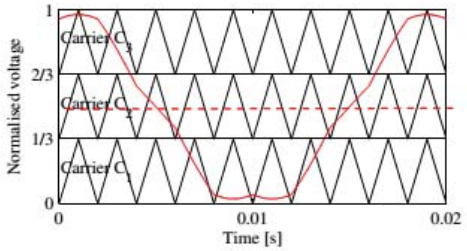


Fig. 5. Phase "a" reference voltage and carrier signals for in-Phase Distribution (PD) PWM [11].

where v_i^* is the reference voltage for i^{th} phase, while C_k are carrier signals. The real gating signals (of) the switches for inverter 1 and inverter 2 are obtained by using relation between gating signals and logical variables A_{ki} that is writen as $S_{2i} = A_{2i}$ and S_{1i} = NOT (A_{1i}) + A_{2i} – NOT (A_{3i}).

Various operation modes can be selected by adjusting the reference offset (the dash line in Fig. 5). At modulation index, $M > 0.7$, the reference offset is set to ½ since the full DC-link is required. At modulation index $0 < M < 0.35$, reference offset is 1/6 hence only one inverter operates in PWM mode while the other inverter is locked at zero vectors. Although improved output voltages can be obtained, the proposed PWM scheme suffers from the overcharged of the capacitor DC-link voltage of one inverter and particularly, PD CB PWM also generates voltage spikes due to the dead-time effect when both inverters are switched at the same time [12]..

Jones et al (2014) developed PWM methods for a four-level five-phase OeW drive using a decoupled modulation technique. The voltage references are apportioned according to modulation index, M, using constrains as expressed at (2). Modulation index defines as comparison of a voltage reference and one half of DC-link voltage, $M = |v^{**}| / (0.5V_{dc})$, where v^{**} is the modulating reference voltage and V_{dc} is the value of the DC-link voltage. At M = 1,0 frequency fundamental of output voltage is set to 50 Hz**.** The individual modulation index, is defines as $M_1 = |v_1^*| / (0.5V_{dc1}$ and $M_2 = |v_2^*| / (0.5V_{dc2})$

$$0 \le M \le 0.35 \begin{cases} M_1 = 3M \\ M_2 = 0 \end{cases} \qquad (2)$$

$$0.35 < M \le 1.05 \begin{cases} M_1 = 1.05 \\ M_2 = 1.05(M - 0.35) \end{cases}$$

It is implied from equation (2) that when M ≤ 0.35, only inverter 1 operates in two-level mode while inverter 2 is locked at zero switching state (11111 or 00000) and when M > 0.35, two inverters operate so that inverter 1 operates at maximum modulation index (M_1=1.05) while inverter 2 operates using modulation index of M_2=1.05(M-0.35). The divided refences then are modulated using the common two-level SVPWM technique with 2-large and 2-medium vectors are selected per sector. This method is named as Un-equal Reference Sharing (URS) method [12].

Since the voltage references are unequaly aportioned, the multi-level inversion is achieved especially when $M > 0.35$ while at $M < 0.35$ inverter works in two-level mode since only one inverter operates. Based on the type of carrier signals of two inverters, two varians of URS PWM schemes are developed. Between the two methods, the URS PWM with the same carrier signals results a better output voltage quality. Both schemes improve the inverter performance compared with the decomposition PWM scheme with equal DC-link voltage for almost all operating regions.

3 The Proposed PWM Scheme

The proposed modulation method adapts the decomposition PWM scheme for the three-level dual-inverter fed OeW five-phase drive [13,14]. It is however, a simple modification is required particurlarly in the higher speed ranges. In the decomposition PWM, the voltage reference mapped in the α-β plane is decomposed into two parts which are alocated for inverter 1 and inverter 2. The voltage reference for inverter 1 is modulated using a single switching state nearest to the tip of the reference while the reference voltage of the inverter 2 is modulated using Space Vector PWM (SVPWM) technique. Realisation of the decomposition PWM scheme using carrier based PWM method is done by modulating inverter 1 at fundamental frequency or switched at zero states (for lower modulation index) while inverter 2 is modulated at PWM mode by comparing the modulation signals of inverter 2 with the high frequency carrier signal. The reference signal of inverter 2 is obtained by subtracting the respective phase of the sinusoidal reference voltage with the phase leg voltage of inverter 1.

The proposed PWM operates in three different operation modes according to the speed range (modulation index). At modulation index, $0.7 < M \le 1.05$, inverter-1 operates at fundamental frequency while inverter 2 operates at PWM mode. The 180° conduction mode is modified by reducing the ON-time duration of both upper and lower switches. The method to generate the gating signals for $0.7 < M \le 1.05$ is shown at upper trace of Fig. 6 and the respective gating signals of phase '*a*' upper and lower switches inverter 1 for M = 1.0 are shown at middle and lower trace of Fig. 6. The gating signal of the upper and the lower switches are governed by using equations (3) and (4).

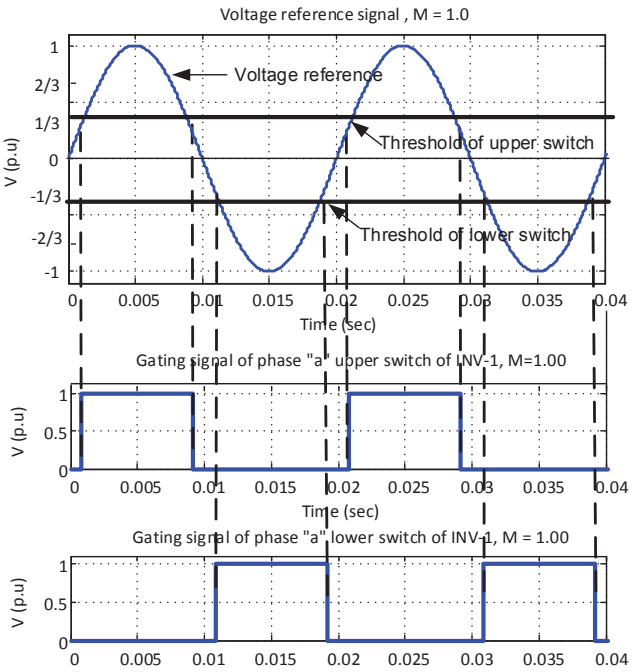


Fig. 6. Gating signals of phase 'a' upper and lower switches for inverter 1, M = 1.0

The equations consist of simple logics that compare the voltage references (v_{rx}) with a particular value of 0.4. For the upper switches, if $v_{rx} > 0.4$, the switches are ON, otherwise the switches are OFF. For the lower switches, if $v_{rx} < -0.4$, the switches are ON, otherwise the switches are OFF.

$$\begin{aligned} &if\ v_r > 0.4 \text{ then } S_{x1(x=a,b,c,d,e)} = 1 \text{ (High)} \\ &else\ \ S_{x1(x=a,b,c,d,e)} = 0 \text{ (Low)} \end{aligned} \tag{3}$$

$$\begin{aligned} &if\ v_{ref} < -0.4 \text{ then } S_{x2(x=a,b,c,d,e)} = 1 \text{ (High)} \\ &else\ \ S_{x2(x=a,b,c,d,e)} = 0 \text{ (Low)} \end{aligned} \tag{4}$$

S_{x1} and S_{x2} for $x = a, b, c, d, e$ are the switching functions of the upper and the lower switches of inverter 1.

It is shown at Fig. 6 that the gating signal of the upper and lower switches are no longer precisely opposed but some delay is now present. When modulation index is reduced, the ON-time duration of the upper and lower switches is also reduced hence the value of the leg voltage of inverter 1 is varied according to modulation index. (The leg voltage that produced using 180° conduction mode is fixed regardless of the modulation index). This is advantageous, not only for improving the quality of the output voltages of converter but also for keeping a balance operation between two inverters hence avoid the increase of the DC-link voltage of inverter 2.

Meanwhile Fig. 7 shows the way to generate the gating signals for inverter 2 at particular $M = 1.0$. The upper trace of Fig. 7 shows that the phase 'a' reference signal of inverter 2 is obtained by subtracting the phase 'a' sinusoidal voltage reference (dash-dot line) and the phase 'a' leg voltage (dashed line). Phase 'a' modulation signal of inverter 2 is achieved by using min-max injection method (equivalent SV-PWM method) as shown in the middle trace of Fig. 7. Comparison of the modulation signal with a triangular carrier signal results phase 'a' gating signal of the upper switch of inverter 2 as shown at the lower trace of Fig. 7. The gating signals of the lower switches are complementary of the gating signals of the upper switches.

At Modulation index, $0.35 < M \leq 0.7$ inverter 1 operates at 180° conduction mode while inverter 2 operates in PWM mode. In this speed ranges, the DC-link voltage of inverter 1 is reduced one half hence an equal ratio of DC-link voltage is now applied. In order to avoid the unbalance operation between two inverters, operation between two inverters is alternated between 180° conduction mode and PWM mode for every cycle of operation [15]. Fig. 8 and Fig. 9 show the gating signals of phase 'a' of the upper switches of inverter 1 and inverter 2 for $M = 0.7$ along with the method to generate the gating signals using carrier based PWM. The gating signals for the other phases are obtained by comparing the consecutive phases of voltage reference with the same triangular carrier signal.

Finaly, at modulation index, $0 \leq M \leq 0.35$, only inverter 2 is activated while inverter 1 clamped at zero switching state (11111 or 00000). Fig. 10 shows the gating signal of upper switches of inverter 1 and inverter 2 respectively at $M = 0.3$. It is clearly shown that inverter 1 is switched off and forming a star-connected of one end of the stator windings that means the two-level inverter single side supply mode is now applied.

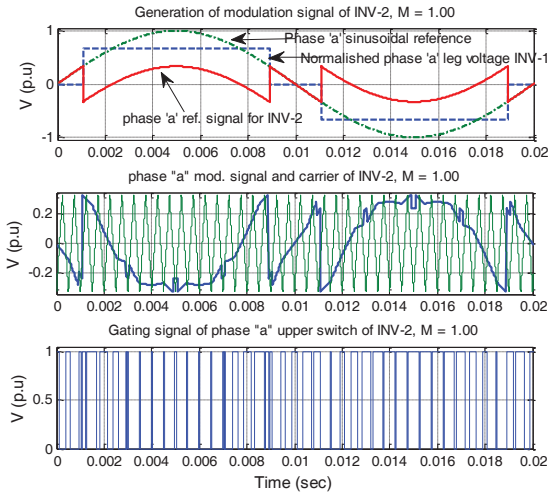


Fig. 7. Generation of phase "a" gating signal upper switch inverter 2, $M = 1.0$

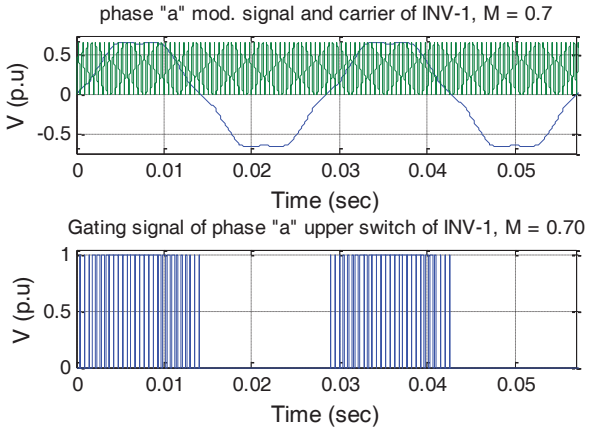


Fig. 8. Generation of gating signals of phase 'a' upper switch of inverter 1, $M = 0.7$

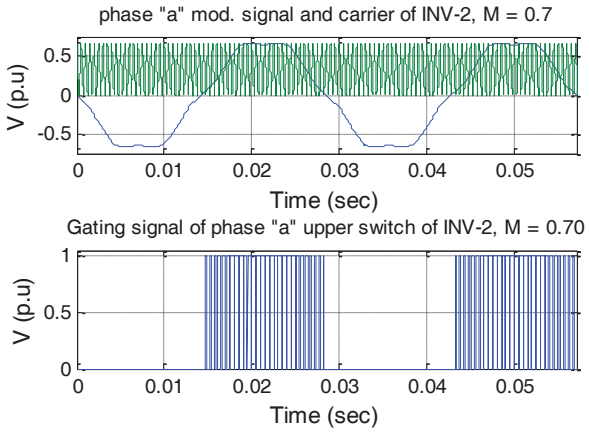


Fig. 9. Generation of gating signals of phase 'a' upper switch of inverter 2, $M = 0.7$

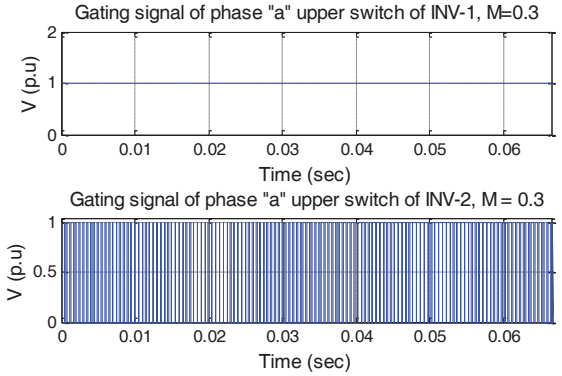


Fig. 10. Gating signals of phase 'a' upper switches of inverter 1 and inverter 2, $M = 0.3$

4 Simulation Results

4.1. Output voltages quality

The proposed PWM scheme is verified using MATLAB / Simulink. The inverters switches are modeled using SimPower Blockset, the gating signals are generated using simulink and a five-phase statis RL load is connected in the mid point of each leg of inverter 1 and inverter 2. The DC-link voltages are set for 400 V : 200 V for $M > 0.7$ and 200 V : 200 V for $M \leq 0.7$. The switching frequency of the PWM inverter is 2 k Hz and the effect of dead-time is neglected.

Fig. 11 - 13 depict the phase '*a*' output voltage of the dual-inverter fed five-phase OeW drives at particular modulation index of $M = 1$, $M = 0.7$, and $M = 0.3$ respectively. The voltage waveforms indicates nearly sinusoidal voltages are successfully achieved. The voltage waveforms consists of 19, 15 and 9 voltage levels for $M = 1$, $M = 0.7$, and $M = 0.3$ respectively that means a four-level, three-level and two-level operation is performed. The harmonics spectra show that the output voltages contain only harmonic at fundamental frequency while the low-order harmonics are shifted at arround multiple switching frequency and its side-band.

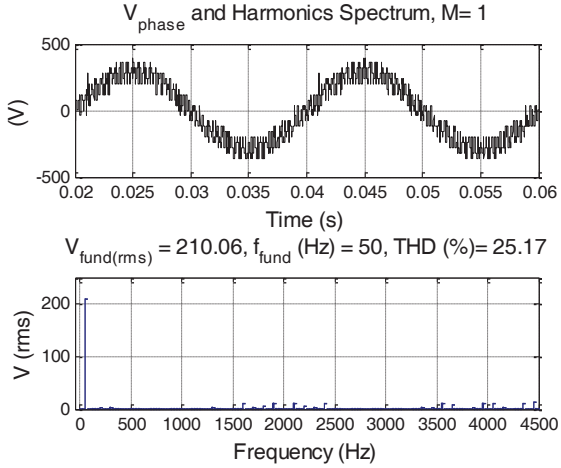


Fig. 11.. Phase "a" output voltage at $M = 1.0$ and harmonics spectrum

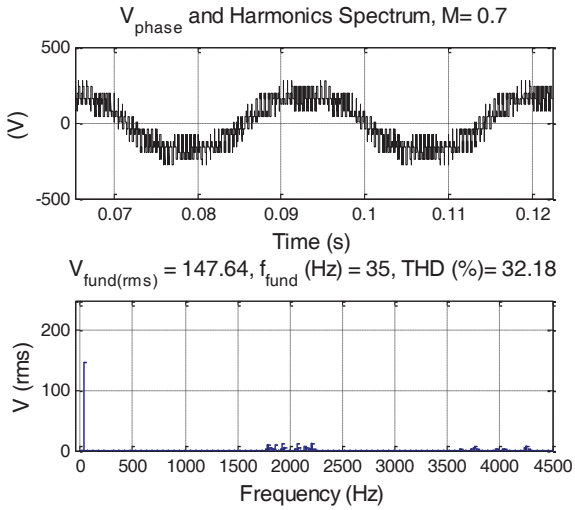


Fig. 12.. Phase "a" output voltage at $M = 0.7$ and harmonics spectrum

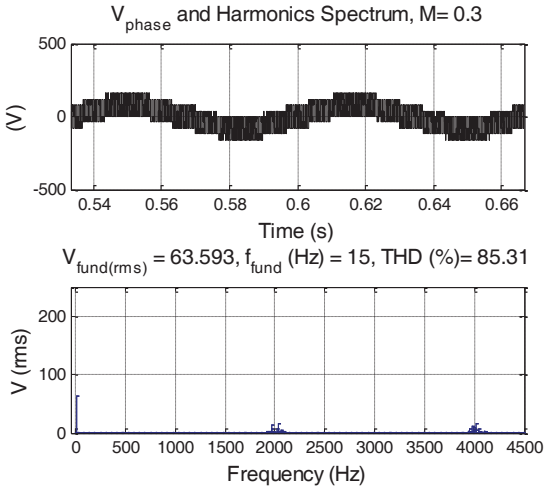


Fig. 13. . Phase "a" output voltage at $M = 0.3$ and harmonics spectrum

Fig. 14 shows projection of the output voltages in the α-β and *x-y* planes for $M = 1$, $M = 0.7$, and $M = 0.3$ respectively. It can be seen that an optimum value of fundamental component that mapped in α-β plane is able to achieve while the unwanted low-order harmonics that mapped in *x-y* plane are sucesfully supressed into a small value. This indicates that the main requirement for controlling a five-phase motor has been succesfuly reached within the proposed modulation startegy.

4.2. THD of the output voltages

In order to further verify the proposed PWM scheme, simulation was repeated from modulation index of 0.05 to 1.05 with 0.05 increaments. THD of the output voltage is noted and presented at Fig. 15. The voltage THD is calculated up to 2000th harmonics as described at equation (5). The value of THD is compared with the THD of the output voltages that are achieved by using the three-level and the previous four-level PWM for the dual-inverter fed OeW five-phase drive.

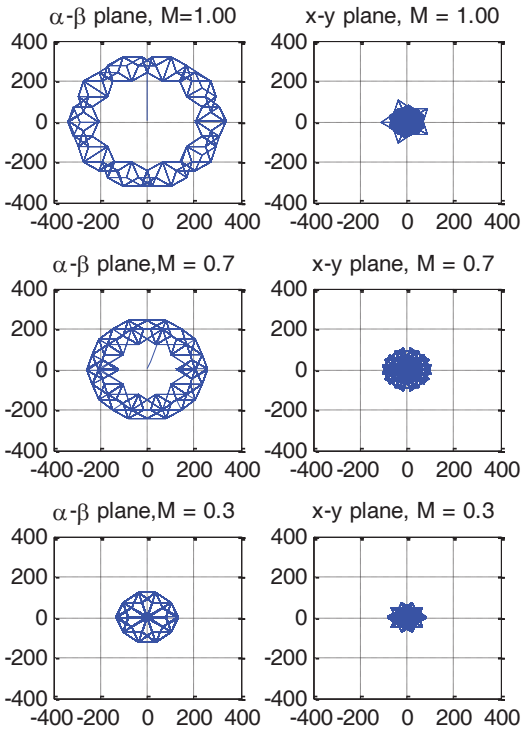


Fig. 14. Projection of the phase output voltage to α-β and *x*-*y* planes for $M = 1.0$, $M = 0.7$ and $M = 0.3$ respectively

$$V_{THD} = \sqrt{\frac{\sum_{n=2,3...}^{2000} v_n^2 - V_1^2}{V_1^2}} \qquad (5)$$

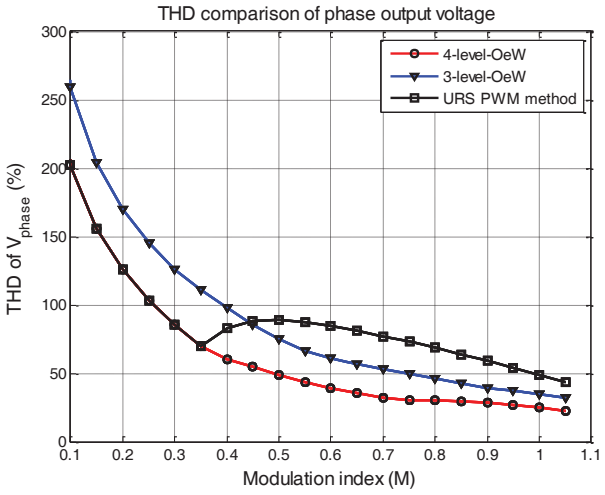


Fig. 15. THD comparison of the various PWM schemes for dual-inverter fed OeW five-phase drives

It is clearly shown at Fig. 15 that the performance of the output voltages is considerably improved for all speed ranges compared with the output voltages that are achieved by the three-level PWM for the dual-inverter fed OeW five-phase drives with equal DC link [16, 17]. The quality of the output voltages is also improved compared to the previous four-level PWM in particular using the URS PWM method as reported at Jones et al (2014) [12] especially for $M \geq 0.35$, while for $M < 0.35$ the performance is exacly the same as the PWM method applied is the same (i.e only one inverter is activated).

4.3. Evaluation of the leg voltages of inverter 1 and inverter 2.

In order to ensure a balance operation between the two inverters, the fundamental value of the phase '*a*' leg voltages of both inverters particuarly for $M > 0.35$ were noted and presented at Table 1. It can be seen from Table 1 that the fundamental value of inverter 1 leg voltages has never exceeded the fundamental value of the output voltages. This indicates that both inverters always supply a positive power to the load for all speed range even at the transition mode from four-level to three-level operation that takes place at $M = 0.71$ (the bold numbers in Table 1). It is also shown at Table 1 that in the range of $0.35 < M \leq 0.7$ both inverters always generate a similar fundamental value in the leg voltages that confirms the ballance operation between two inverters is able to achieve. It can be concluded that the proposed PWM scheme has a good capability to maintain the value of the DC-link voltage at the certain value. It is however, a further investigation is required to suport the finding i.e by evaluating the usage of the voltage space vectors for various modulation index.

M	V_{out} (V)	$V_{legINV1}$ (V)	$V_{legINV2}$ (V)
1.05	221.84	165.5	56.3
1.00	210.77	164.08	49.65
0.90	190	160.4	38.1
0.8	168.64	155.07	13.6
0.75	158.6	151.5	7.26
0.71	**148.11**	**146.6**	**1.73**
0.70	148	73.7	74.2
0.6	126.8	63.17	63.6
0.5	105.7	52.7	53
0.4	84.54	42.1	42.1
0.36	75.85	37.7	38.1

Table 1. Rms fundamental value of phase 'a' output voltage, phase 'a' leg voltages of inverter 1 and inverter 2 for various modulation index.

5. Conclusion

A new PWM scheme for a four-level dual-inverter fed OeW five-phase induction motor drive is presented in this paper. The developed PWM method adapts the decomposition PWM scheme for the dual-inverter fed five-phase drives with equal DC-link voltage. The proposed PWM method has been verified using MATLAB/Simulink. The results show that the quality of output voltages are significantly improved in comparison with the output voltages that are generated using the three-level PWM, and the previous four-level PWM schemes. The proposed PWM scheme is also inherently able

to ensure a balance operation between two inverters hence avoid the overcharged of DC-link voltage. One drawback of the proposed method is that the aditional circuit is required to reduce the value of DC-link voltage of inverter 1 at particular range modulation index, $0.35 < M \leq 0.7$

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