Simple Carrier Based Space Vector PWM Schemes Of Dual-Inverter Fed Three-Phase Open-End Winding Motor Drives With Equal DC-Link Voltage

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Abstract— **Dual-inverter fed open-end winding (OeW) motor drives has been subject of research for last 2 decades. The structure offer many advantages over the conventional multi-level counterpart. In line with the potential feature the dual-inverter fed OeW drives require a proper modulation method to obtain improved quality voltages. The existing PWM methods are based on the space vector approach which involves many steps of procedure hence it is formidable. This paper proposes four PWM schemes for the dual-inverter fed OeW 3-phase motor drives. The PWM schemes are developed by dividing the reference in a certain way and they are modulated in the same or different PWM technique. Realization of the PWM schemes was done by the Carrier Based PWM. Simulation results show that the Mixed Switching Frequency (MSF) PWM provides the best output voltage quality among the PWM schemes especially for $M > 0.575$. Further investigation also reveals that the performance of PWM scheme relates with the utilized voltage vectors. Here, the MSF PWM is able to select the most effective voltage vectors among the 19 available vectors (64 switching states).**

Keywords—Dual-inverter fed, Open-end Winding, Carrier Based PWM, Mixed Switching Frequency

I. INTRODUCTION

Multi-level inverter has been proven provides better quality output voltages over the two-level inverter. Various topologies of multi-level inverter have been developed over decades. Conventional multi-level inverter adds more power switches in series connection and usually used to supply the machine from one side (the neutral point of machine is star connected). Multi-level inverter can be in form of Neutral Point Clamped (NPC), Diode Clamped Inverter or cascaded H-Bridge Inverter. [1]. Lately, dual-inverter fed open-end winding motor drive is introduced by Stemmler and Gugenbach in 1993 [2]. In the dual-inveter fed, the neutral point of the machine is opened and allowing the motor suplied from both sides. Fig. 1 shows the schematic diagram of dual-inverter fed 3-phase OeW motor drive. The dual-inverter fed structure is advantageous. The circuit is simple and potencial to achieve three or four level operation by varying the ratio of DC-link voltage [3,4]. In addition, the dual-inverter fed structure contains higher number of voltage vectors which are generated by combination of switching states of the two inverters. Hence, with the proper PWM method, the higher switching combination can be optimized to achieve a better output voltage. In the contrary, con ventional multi-level inverter (NPC) formed from complicated circuit and suffers from drawback of unbalance of capasitors voltage hence it requires particular PWM scheme with capasitor voltage balancing technique [5,6].

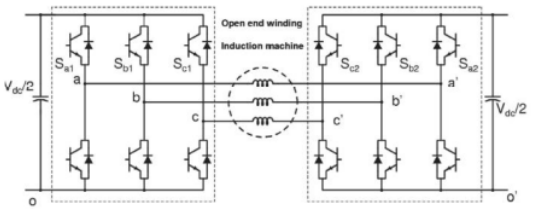


Fig. 1 Dual two-level inverter fed Open-end Winding three-phase motor drives

Despite of the advantages offers in the dual-inverter fed structure, the development of suitable modulation strategy is more complicated than two-level inverter. Various PWM methods of dual-inverter fed 3-phase motor drive has been developed. The available modulation strategies is mainly focused to achieve a multi-level operation hence reduce the harmonics content (THD), minimizing the zero squence current / Common mode voltage (CMV), and simplify the procedures [7-11]. The available PWM methods are developed based on the space vector approach where the prosedures are formitable.

This paper proposes four PWM methods for the dual-inverter fed 3-phase OeW motor drive with equal DC-link voltage. In order to reduce complexity, the PWM methods are developed by dividing the voltage references to inverter 1 and inverter 2. The PWM signals are generated using carrier based method similarly as applied in [12]. The first PWM scheme is developed by equaly dividing the reference and then modulating using space vector equivalent carrier based PWM. The second and the third PWM are developed by deviding the reference unequaly according to the value of modulaton index. The fourth PWM is done by equaly dividing the reference but the level of carrier signal of two inverters are modified. The proposed PWM schemes were verified using Matlab / Simulink. The results are presented and analished in term of output quality / THD and the vector utilisation.

II. VOLTAGE SPACE VECTOR OF DUAL-INVERTER FED OEW MOTOR DRIVES

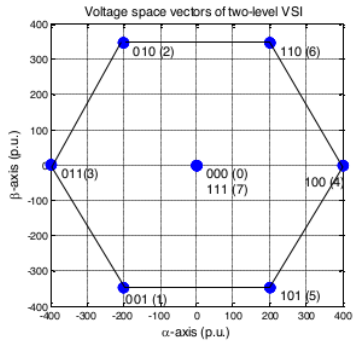
Voltage space vectors of a two-level VSI is governed by using equation (1). The value of the voltage vectors depands

on the switching state condition of the upper (or the lower) switches of the two-level VSI. There are 7 voltage space vectors for the two-level inverter which are generated by 8 (2^3) switching states as shown in Fig. 2 (a) [13]. Similarly, voltage space vectors of the dual-inverter fed structure is developed by switching state combination of inverter 1 and inverter 2 and governed by equation (2) [13]. Combination of 64 (8x8) switching states results 19 voltage space vectors as shown in Fig. 1 (b) In Fig. 2 (b) the labels in decimal number indicates the switching state combination when it is converterd into binary value. The first number relates to switching states for inverter 1 and the second number relates to switching states for inverter 2.

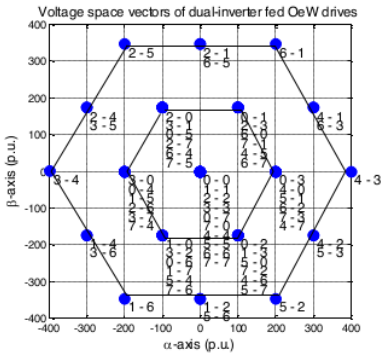
$$\underline{v}_{\alpha\beta} = v_\alpha + jv_\beta = 2/3(v_{aO}(t) + v_{bO}(t)e^{j2\pi/3} + v_{cO}(t)e^{j4\pi/3}) \quad (1)$$

where $v_{xO}(t)_{(x=a,b,c)}$ = instantanous load phase voltages

$$\underline{v}_{\alpha\beta_{(DUAL)}} = \underline{v}_{\alpha\beta(INV1)} - \underline{v}_{\alpha\beta(INV2)} = 2/3\{(v_{aO}(t) + v_{bO}(t)e^{j2\pi/3} + v_{cO}(t)e^{j4\pi/3}) - (v_{a'O'}(t) + v_{b'O'}(t)e^{j2\pi/3} + v_{c'O'}(t)e^{j4\pi/3})\} \quad (2)$$



(a)



(b)

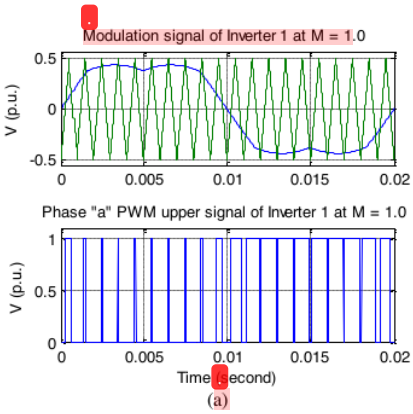
Fig. 2. Voltage space vectors of ; (a) Two-level VSI. (b) Dual-inverter fed 3-phase OeW motor drive.

It is shown in Fig. 2 (b) that combination of the 64 switching state generates 10 zero vectors (locates in the origin of the plane), 6 vectors in the inner decagon generated by 36 switching combinations, 6 vectors in the outer decagon generated by 12 switching combinations and the other 6 vectors in the outer decagon generated by 6 swtching combinations.

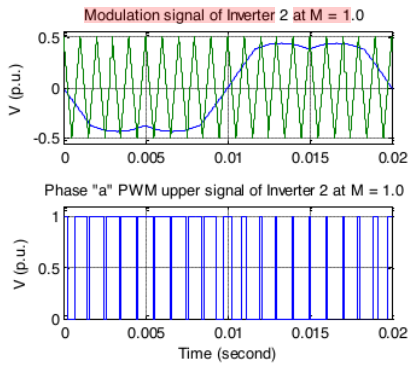
III. Proposed Carrier Based PWM Schemes for Dual-Invrter Fed 3-Phase OeW Drives

A. Equal Reference Divison PWM Scheme

The first PWM scheme is developed by dividing the voltage references equaly and modulated using carrier based space vector equivalent technique. The modulation signals are obtained by injecting the zero squence signal into the sinusoidal reference signals. The PWM signals are generated by simply comparing the modulatin signals (V_m) and the triangular high frequency signal (V_c). By using a simple logic, i.e if the $V_m > V_c$, PWM pulse is high (1) and if $V_m < V_c$ the pulses are low (0) or vice versa the PWM pulses are generated. Fig. 3 shows the phase a upper switches PWM signals for inveter 1 and inverter 2 along with the comparison of the modulation signal and carrier signal. the modulation scheme is termed as Equal Reference Division (ERD) PWM Scheme



(a)



(b)

Fig, 3, PWM generation of the ERD scheme for; (a) phase "a" upper switch inverter 1, (b) phase "a" upper switch inverter 2 at $M = 1.0$.

B. Unequal References Division PWM Scheme

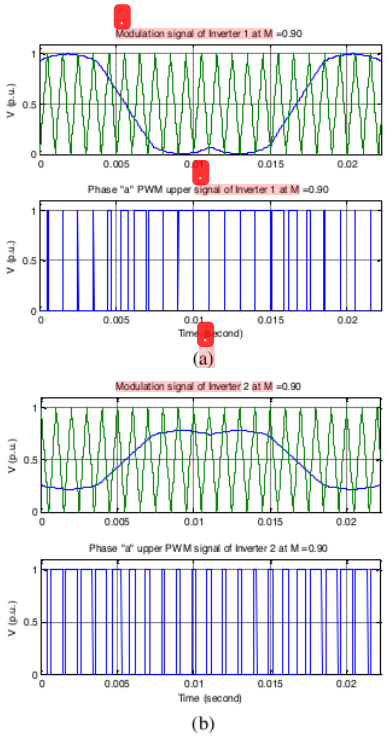
The second PWM scheme for the dual-inverter fed OeW fhree-phase motor drive is also done by dividing the reference voltages proportionally according to the value of the

Modulation index. The proportion of the references are governed by equation (3).

$$\begin{cases} 0 \le M \le 0.575 & \begin{cases} M_1 = 2M \\ M_2 = 0 \end{cases} \\ 0.575 < M \le 1.15 & \begin{cases} M_1 = 1.15 \\ M_2 = 2(M - 0.575) \end{cases} \end{cases} \quad (3)$$

M is defined as ratio of the inverter output voltage and the DC-link voltage. The maximum valus of M for three-phase motor drives is 1.15. Equation (3) governs the references so that at $M > 0.575$, the reference voltages of inverter 1 (M_1) is kept at maximum value while reference voltages of inverter-2 (M_2) reduces proportionaly in line with the reduction of M. At $M \le 0.575$, the reference voltages only alocated to inverter-1 and they are modulated using two-level SVPWM while inverter-2 is locked at switching state of (111) or (000). This condition reverts the dual-inverter fed sistem into two-level single-sided fed mode. The divided references are then modulated using the carrier based Space Vector equivalent PWM. This modulation scheme is termed as Unequal Reference Division (URD) PWM Scheme.

Fig. 4 shows the comparison phase "a" modulation signal and carrier signal along with the phase "a" upper switch PWM signal of inverter 1 and inverter 2 for particular M = 0.90

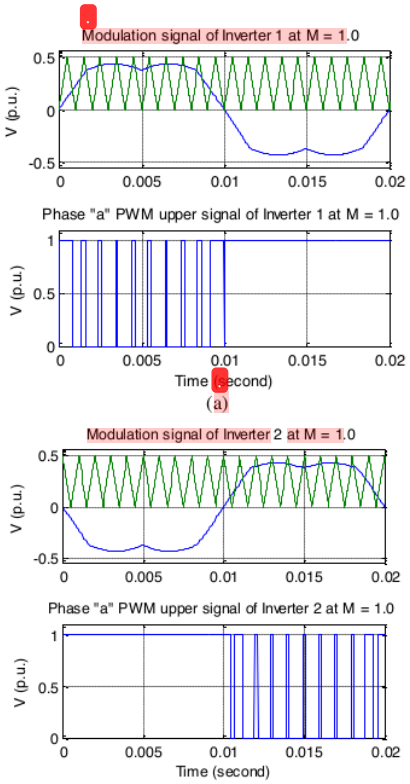


Fig, 4, PWM generation of the URD scheme for; (a) phase "a" upper switch inverter 1, (b) phase "a" upper switch inverter 2 at M = 0.9.

According to the type of the carrier signal the URD scheme can be clasified into URD1 PWM (where the carrier signal of inverter 1 is in same phase with the carrier signal of inverter 2) and URD2 PWM (where the phase opposition of the carrier signal is applied).

C. Mixed Frequency Switching (MFS) PWM Scheme

The four PWM scheme is also developed by spliting the reference voltages, but they are modulated with diferent PWM technique. At $M > 0.575$, the reference voltages for inverter-1 are modulated using 180° conduction mode while inverter-2 are modulated using PWM mode. Here, the modulation signals of inverter-2 are obtained from resultant of the phase sinusoidal reference voltages and the respective phase output voltages of inverter-1. At $M \le 0.575$ only one inverter is moduated using SVPWM scheme while inverter-2 is switched off (locked at switching state of (111) or (000)). This scheme is named Mixed Frequency Switching (MFS) PWM scheme since in this method, one inverter is operated in slow frequency switching (fundamental frequency) and one inverter is operated in high frequency switching (PWM). The drawback of MFS PWM scheme is that unbalance number of switching commutaion between two inverters. Hence, in order to balance the number of switching comutation in one cyrcle the role of inverters is alternated between slow and fast switching operation.



Fig, 5, PWM generation of the MSF PWM scheme for; (a) phase "a" upper switch inverter 1, (b) phase "a" upper switch inverter 2 at M = 1.0.

The alternated PWM scheme is realised by applying carrier based method i.e by shipting the level of the carrier signal of inverter 1 and inverter 2 as shown in Fig. 5. It is

shown in Fig. 5 that comparison of the modulation signals and the carrier segnals results switching signals which consist of fast switching frequency (PWM mode) and slow switching frequency in one circle of operation.

IV. Results and Discussion

The proposed PWM methods is verified using Matlab / Simulink. The switches are developed using *Simpower BlockSet* and the PWM signals genererated using Simulink. Both inverters apply 300 V DC-link input. Deadtime effect is ignored in the simulation. The sistem is set to have fundamental frequency output of 50 Hz at $M = 1.0$.

A. Output Voltage Waveform

The generated phase "a" output voltages for various modulation indeces of $M = 0.8$ (40 Hz) and $M = 0.5$ (25 Hz) are shown at Fig 6 and to Fig. 7 respectively. It is shown in the Fig. 6 that the voltage waveforms contains of 5 voltage levels for ERD PWM and 9 voltage levels for URD and MSF PWM (multi-level operation). The harmonics spectra reveals that the rms of fundamental voltages are almost 170 V which are close to the expected value. The spectra also show that the nearly sinusoidal output voltages are achieved which is indicated by a small amount of low order harmonics component since they are shipted into arround multiple switching frequency and it side band. Further, at $M = 0.5$ (Fig, 7), all PWM schemes operate in two-level operation. The voltage waveforms contain 5 voltage levels. In this condition the URD and MSF PWM only activate one inverter and supply the machine from one side only (except of the ERD PWM scheme, still feed the machine from two sides).

B. Performance of Output Voltage

In order to show the whole performance of the proposed PWM schemes, simulation is repeated for all modulation indeces with 0.05 increament steps. The THD value of the output voltages for $0.1 < M \leq 1.15$ is presented in Table 1 and THD comparison of the output voltage for various modulation methods is shown in Fig. 8.

It can be seen form Fig. 8 that the performance of the ERD PWM is exactly the same with the two-level VSI. The quality of output voltages is improved by the URD and the MSF PWM for all modulation indices. The value of THD also reveals that URD with the same phase carrier provide a better performance than the URD with opposite phase of carrier. Among proposed PWM, the MSF PWM generates the best output voltage quality especially at $M > 0.575$ as shown in the Fig 8. While for $M \leq 0{,}575$ the URD and MSF PWM performs the same voltage quality since the PWM schemes operate only one inverter.

C. Analysis of Voltage Space Vectors Utilisation

Subsequently, relation of the utilished the voltage vectors (switching states) with the quality of the output voltages is analyshed.. A Matlab program and simulink model were developed to examine the activated voltage vectors among the PWM schemes. Fig. 9 reveals the utilished vectors for various PWM schemes.

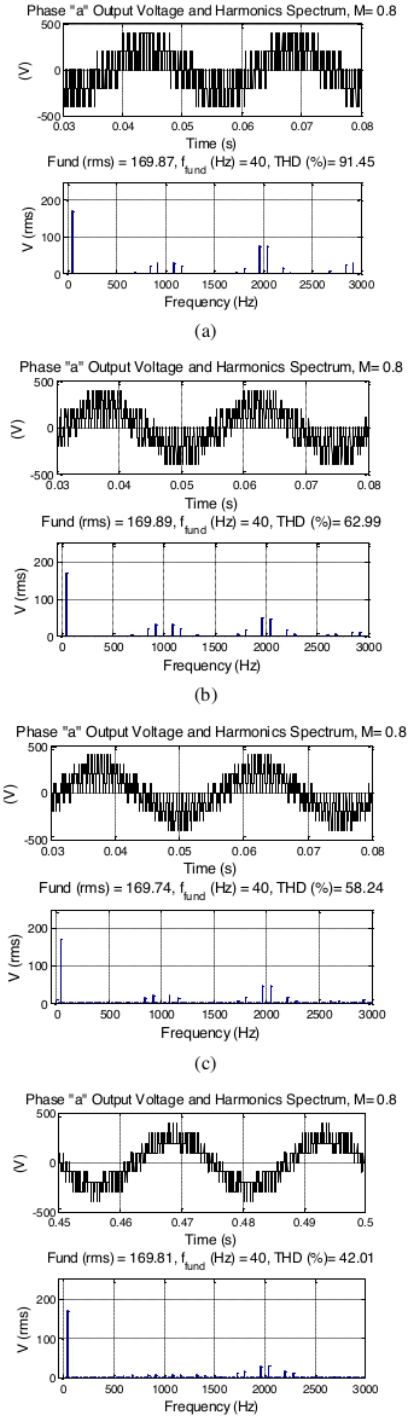
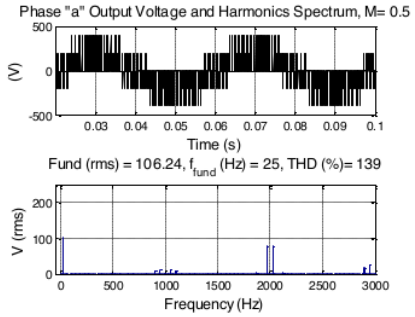
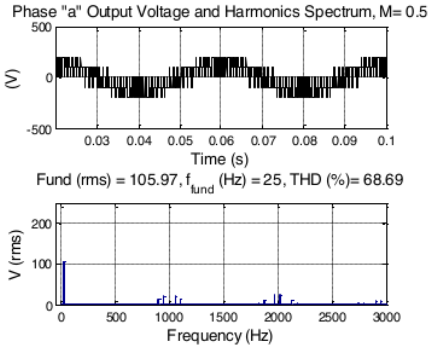


Fig. 6. Output Voltage at $M = 0.8$ for; a). ERD PWM, b). URD1 PWM (opposite carrier). C). URD2 PWM (same carrier), d). MSF PWM



(a)



(b)

Fig. 7 Output Voltage at $M = 0.5$ for; a). ERD PWM, b). URD1 PWM (opposite carrier).,URD2 PWM (same carrier), d). MSF PWM Scheme

TABLE I. THD COMPARISON OF THE OUTPUT VOLTAGE FOR VARIOUS PWM SCEME

M	THD of Output Voltage in %			
	ERD	URD1 (Opposite Carrier)	URD2 (Same Carrier)	MSF
1.15	52.88	52.76	32.74	27.45
1.10	57.86	54.58	37.4	30.25
1.05	63.03	56.75	42.37	32.26
1.00	68.45	58.42	46.22	35.26
0.95	73.77	60.75	49.49	37.97
0.90	79.55	60.99	52.04	39.25
0.85	85.56	62.45	56.01	40.84
0.80	91.35	62.99	58.23	42.11
0.75	97.8	62.95	59.38	43.18
0.7	105.1	62.24	60.62	44.23
0.65	112.1	60.43	59.39	45.84
0.6	121	56.44	56.29	49.28
0.55	129.5	57.93	57.93	57.93
0.5	139	68.69	68.69	68.69
0.45	150.4	79.8	79.8	79.8
0.4	163	95.3	95.3	95.3
0.35	178.5	104.6	104.6	104.6
0.3	198.5	120.9	120.9	120.9
0.25	221.8	139	139	139
0.2	252.2	163.1	163.1	163.1
0.15	295.2	199	199	199
0.10	364.8	252.3	252.3	252.3

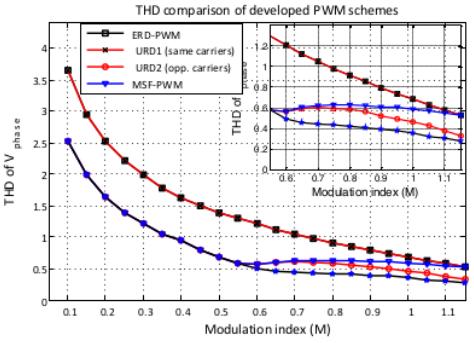
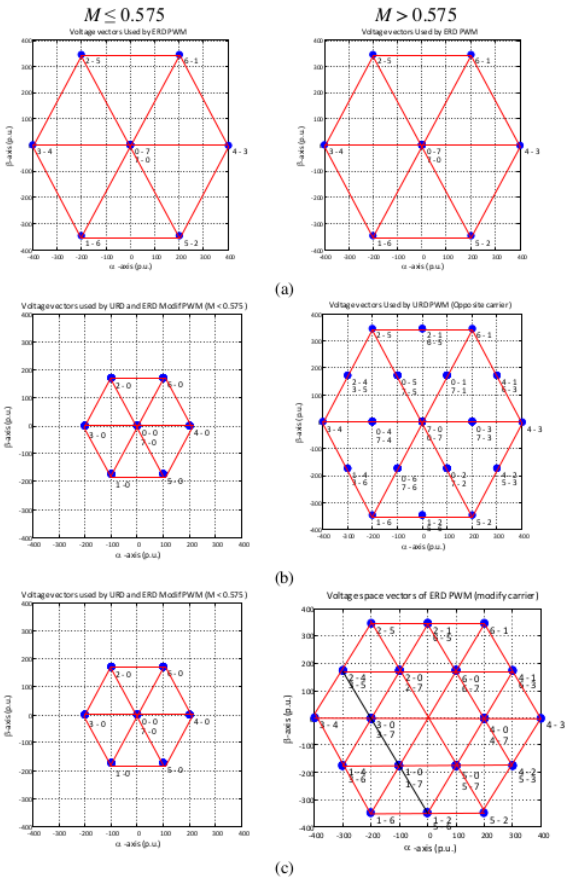


Fig. 8. Output voltage quality comparison of the developed PWM schemes



(a)

(b)

(c)

Fig. 9 The utilished voltage vector for (a) ERD PWM, (b) URD PWM and (c). MSF PWM

It can be seen in the Fig. 9 (a) that the ERD utilizes only 7 voltage vectors (8 switching states) from the 19 vectors (64 switching states). The utilished vectors are the same and remains the same for the change of M. The used voltage vectors in ERD PWM scheme is the same as the vectors in

the two-level inverter, hence the performance of ERD PWM scheme is the same with the two-level inverter.

Subsequently, the MSF PWM and URD PWM utilise different set of vectors according to the value of modulation index. At $M \leq 0.575$, only 7 vectors in the inner decagon (8 switching states) are used, i.e {0-0, 4-0, 6-0, 2-0, 3-0, 1-0, 5-0 and 7-0}. The switching combination operates the second inverter is locked at (000) state. While at $M > 0.575$ the URD PWM, activates all available voltage vectors in the plane including the zero vectors (Fig. 9 (b)). However, the MSF PWM selects wisely the voltage vectors where only 12 vectors are utilished among the 19 vectors (Fig. 9 (c)). At $M > 0.575$, the MSF PWM does not utilises the zero vectors that causes the better quality output which is proven by the waveform of the output voltage and the value of THD.

V. Conclusion

This paper presents four PWM schemes for the dual-inverter fed OeW 3-phase motor drives. The developed PWM schemes are developed by spliting the voltage references and then they are modulated using the same or different PWM strategy. The schemes are simply realished by using an equivalent carrier based SVPWM method. Simulatation results show that the URD and MSF PWM schemes are able to achieve the multi-level operation particularly at $M > 0.575$ hence the output voltage quality improved compared with the ERD PWM scheme (two-level inverter PWM). While at $M \leq 0.575$, the quality of the output voltage also improved compared than two-level inverter since the DC-link voltage applied is reduced by one half. Among the developed PWM schemes, the MSF PWM provides the best THD especially for $M > 0.575$. The quality of the output voltage relates with the utilished voltage vectors. It is revealed that the MSF PWM enables utilises the most proper voltage vectors among the proposed PWM schemes.

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