by Ginarsa I Made

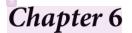
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Abstract. High voltage direct current (HVDC) transmission is a better prospect choice compared to high voltage AC transmission. The HVDC is able to apply higher voltage level and without any reactive power losses. By supporting power electronic technology, the HVDC is simpler and cheaper to be realized. So, the problem in the HVDC system is how to control power flow in rectifier converter device effectively. In this research, regulating of firing delay angle is proposed by ANFIS-based controller (ANC) in 12-pulse rectifier. The ANC is applied because computation of the ANC is more effective than Mamdani fuzzy controller computation. The ANC is trained by data-learning in off-line mode. In normal operation, the maximum transmitted power by the HVDC is on the value of 1.0 pu with voltage and current DC at 1.0 pu when the firing delay angle at 26°. Also, the ANC is able to compensate temporary short-circuit fault.

Keywords. ANFIS, controller, firing delay angle, HVDC, rectifier.

I. Introduction

High voltage direct current (HVDC) transmission system is usually used to deliver bulk of electric power over a long distance area by overhead conductors or submarine cables. The HVDC system has several advantages compared to high voltage alternating current (HVAC) system such as: location of electric power production are very far from location of consumer, long distance HVDC system do not need reactive power compensation as required by long distance of the HVAC system, to make an asynchronous interconnection and allows more capacity of power to be transmitted/delivered [1] [2]. Also, for a given conductor cross section, the HVDC transmission system can carry more current through this conductor compared to a conventional HVAC system[1].

In order to improve the performance of the HVDC system, some control schemes are applied to its such as: A feedback loop with PI controller is applied to the HVDC. The controller is able to mitigate voltage fluctuation during disturbing condition [3]. Also, PI controller is used to multi-infeed high voltage direct current (MIHVDC). Modified transfer function of HVDC also is introduce with small signal analysis based on linearisation model. Parameters of the PI controller in MIHVDC are optimized using genetic algorithm. The MIHVDC are equipped by PI controller and the optimized parameters are robust during fault condition [4].

Analytical method to calculate the efficiency of two and three-level VSC with average and root mean square of converter current is used to the HVDC system. This method is applied to estimate the losses of DC cable, coupling transformer, AC harmonic filter and conduction - switching at the converter. The analytical method and measuring software technique are compared in order to validate of the results [5]. Moreover, power flow strategy with multi-objective optimization for multi-terminal HVDC grid [6] is done by Carrizosa et al. Line commutated rectifier (LCC) and modular multi-level converter (MMC) are applied in hybrid HVDC topology to clear DC fault. Where, the LCC is adopted as rectifier side and the 2 (two) MMC moduls are adopt as inverter side. This topology is able to block current fault path by alpha-retard (α-retard) of the LCC and high power diode. Also, the system is able to restart after clearance of transient DC line fault [7]. A novel rapid protection whole-line principle to protect the HVDC transmission lines using oneend voltage signal was proposed in [8]. Where, this proposed protection method works by analysing measured voltage of the electric network to identify and distinguish between internal or external faults. Moreover, the proposed method operates rapidly, selectively and with high accuracy, under different fault conditions. Natural frequency of distributed parameter line model is applied to determine the fault location on light HVDC system [9]. Using spectral analysis of current by the prony algorithm, a short data window is sufficient to detect the natural frequency and fault location accurately. It is found that the accuracy of fault location over entire HVDC transmission line is not affected by fault resistance and fault type.

Some intelligent control such as: Neural network (NN), fuzzy and neuro-fuzzy control are applied successful in electrical and other engineering fields to replace the function of conventional control scheme in recent years. Proportional integral derivative-static var compensator (PID-SVC) based on recurrent NN has been applied to control chaos and voltage collapse in critical loading of a power system [10]. Moreover, ANFIS-based composite controller-SVC and PID-loop have been applied to control chaos, voltage collapse, and to regulate the load voltage at load bus. In this control scheme, the load bus is varied. In order to maintain the load voltage on the setting value, the reactive power compensation is provided by the SVC [11] [12]. ANFIS controller is applied to control and fault identification in converter of HVDC system. Where, this controller is able to improve dynamic response of the system [13]. Furthermore, ANFIS-based power system stabilizer has been applied to improve the stability of single machine based on feedback linearisation [14]. In this research, we focus on controlling rectifier of HVDC using ANFIS-based controller to replace the conventional controller. This paper is organized as follows: High voltage direct current (HVDC) is described in Section II. ANFIS-based rectifier controller design is detailed in Section III. Next, simulation result and analysis are presented in Section IV. And, the conclusion is provided in the last section.

II. HVDC Transmission Model

The advantage of HVDC is the ability to control the transmitted power rapidly. Proper design of the HVDC control is essential to ensure satisfactory performance of the overall AC/DC transmission systems [15]. Some aspects of power flow control in HVDC using flexible AC transmission system are described in [16] [17].

Consider a DC transmission system to be compared with a 3-phase AC system transmitting the same power, having the same percentage losses and using the same size conductor. Where the DC system is considered to have 2 (two) conductors at V_d to earth. These formulas are as follows [1]: Power in the AC system ($P_a = 3E_{ph}I_L$ assumed that $\cos \phi = 1.0$), power in the DC system ($P_d = 2V_{dL}I_d$), AC losses ($3I_L^2R$) and DC losses ($2I_d^2R$). Equating line losses,

$$3I_L^2R=2I_d^2R$$

Or

$$I_d = (\sqrt{2}/\sqrt{3})I_L$$

equating powers,

$$V_{dL} = (\sqrt{3}/\sqrt{2})E_{ph}$$

where E_{ph} , I_L , P_a , V_{dL} , I_d , P_d and R are the AC voltage phase to neutral, AC line current, 3-phase AC real power, DC voltage, DC current, DC power and line resistance, respectively.

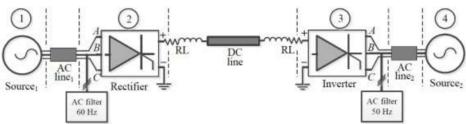


Fig. 1. Model of HVDC transmission system

The HVDC model in this research is taken from [18] and is shown in Fig. . 1. The system consist of 4 buses, step-up/down transformer, 3-phase rectifier/inverter, R_L series branch and 300 km long HVDC transmission. Bus parameters are as follows: Bus 1 consist of AC source with third harmonic, 5000 MVA equivalent, 500 kV, 80° , 60 Hz. Bus 2: (Capacitor bank + 11^{th} + 13^{th} + 24^{th} harmonic filters)×150 MVAR and 3-phase rectifier. Bus 3: Three-phase inverter and 150 MVAR×(capacitor bank + 11^{th} + 13^{th} + 24^{th} harmonic filters). And, Bus 4: AC source with third harmonic, 1000 MVA equivalent, 345 kV, 80° , 50 Hz. Branch parameters: AC line 126.07 Ω and 48.86×10^{-3} H. The transmission DC line: 6.5Ω , 1.2376 H and 4.32×10^{-6} F. And, the transmission AC line 2: 6.205Ω and 13.96×10^{-3} H.

III. ANFIS-Based Control Design

Rectifier Converter and Its Controller

Rectifier converter is very important in HVDC system, that the rectifier converter is used to convert alternating current (AC) to direct current (DC). Therefore, the DC will be transmitted from sending-end to receiving-end through HVDC transmission system. Fig. 2 shows the 12-pulse firing controller unit of the rectifier converter. The controller unit produced $Pulse_Y$ —R to trigger the respective thyristor-gate at 3-phase $A_yB_yC_y$ in star (Y) connected. Also, this controller unit produced $Pulse_D$ —R to fire respective thyristor-gate at 3-phase $A_dB_dC_d$ in delta (Δ) connected. Moreover, the voltage/current from the both star and delta connected were used to generate DC voltage (V_{dL} —R)/current (I_d —R) in the DC side of the rectifier. In order to regulate the level of voltage/current rectifier converter is proper to appropriate of demand side needed, it is convenient to provide this rectifier converter by the controller unit.

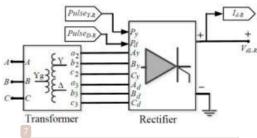


Fig. 2. Diagram block of the HVDC rectifier

The main function of rectifier controller unit is to produce firing delay angle (α_{ord}) signal. This signal is fed to the 12 pulse firing control of the respective thyristor-valve in bridge converter. So, the 12-pulse firing controller generates trigger pulse, that this trigger pulse is used to on/off the thyristor-gate. Furthermore, this controller also produces two other output signals such as: Reference current (I_{dref}) and mode operation (Mode) of rectifier. The diagram block of conventional rectifier controller is shown in Fig. 3(a). Reference current (I_{dref}) is used as the target current level of rectifier, where the DC line current (I_d) should follow the (I_{dref}) on every time. And, the control mode is used to classify the operation of the rectifier into Mode 0: blocked mode, 1: current, 2: voltage, 3: α_{min} , 4: α_{max} , 5: forced α and Mode 6: γ mode.

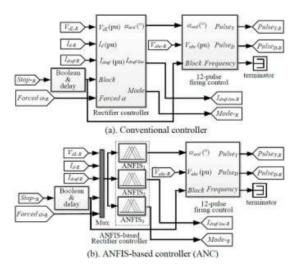


Fig. 3. Diagram block of 12-pulse rectifier controller

Training of ANFIS-based Controller

Before ANFIS-based controller (ANC) is applied to the HVDC converter, that the ANC is trained in some training processes. The data that used on training process were obtained by simulating the conventional controller. The conventional controller is shown in Fig. 3(a). On this training process, a 4000-data point was used to learn the ANFIS controller. Input of the ANC was 5 (five) input variables such as: V_{dL} , I_d , I_{dref} , block and forced α . Three (3) ANFIS models were used to implement the rectifier controller such as: ANFIS₁, ANFIS₂ and ANFIS₃. The output of respective ANFIS model were the α_{ord} , I_{dref} –R and mode operation of the rectifier (Mode R). The ANC diagram block of the rectifier converter is shown Fig. 3(b).

In this research only the ANFIS₁ topic is described, meanwhile ANFIS₂ and ANFIS₃ are not discussed. Structure of ANFIS controller was built by 5 (five) inputs Sugeno fuzzy model and 1 (one) output as shown in Fig. 4(a). The training process was conducted in off-line session and subtractive clustering method was used to generate fuzzy inference system (FIS). In this session, some parameters such as: Range of influence = 0.5, squash factor = 1.5, accept ratio = 0.5 and reject ratio = 0.15 were taken. Every input variables were consist of 4 (four) Gaussian membership functions, the I_d input was taken as example and shown in Fig. 4(b). After some training processes were conducted, control surface of respective input-output controller was obtained automatically. This session produced ten (10) sets of input-output control surface of the ANC. An example of the input-output control surface is a DC line voltage-DC current-firing delay $(V_{dL}-I_d\alpha_{ord})$. So, this control surface is shown in Fig. 4(c).

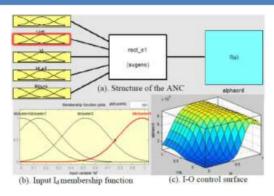


Fig. 4. Parameters of the ANFIS-based controller (ANC).

Table 1. Performance Of Anfis Controller At Normal Operation

period/	t_0	t_1	t_2	t_3	t_4
observed	(.02 s)	(0.3 s)	(1.4 s)	(1.6 s)	(1.7 s)
α_{ord}	90.0-	92.0-	26.0-	166.0	166.0
(°)	92.0	30.0	40.0		
$V_{ph[p-p]}$	1.135	1.135-	0.96-	1.135	1.135
(pu)		0.96	1.135	0.99	
$I_{L[p-p]}$	0.5	0.5-	11.9-	0.0	0.0
(pu)		11.9	0.0	111	
V_{dL}	0.05-	1.06-	1.0-	0.96-	-0.25
(pu)	1.06	1.0	0.96	-0.25	
I_d	0.04	.04-	1.0-	0.0	0.0
(pu)	ROWHER OF	1.0	0.0	0.000	
P_d	0.0-	0.0242-	1.0-	0.0	0.0
(pu)	0.0242	0.0	0.0		

IV. Simulation and Analysis

To demonstrate the performance and applicability of the proposed controller, the HVDC system equipped by that controller was examined using Matlab/Simulink 7.9.0.529 (R2009b) [19] on an Intel Core 2 Duo E6550 233 GHz PC computer and windows 7 64-bit (win64) operating system. The simulations were done as follows:

A. Performance of ANFIS-based Controller at Start/stop and Ramp-up/down

Scenario 1: the HVDC system was operated with some parameter as follows: At start-up both converters were deblocked and ramped-up to the minimum current (minimum steady-state current reference, MSCR) at 0.1 pu with an adjustable rate (start ramp rate, SRR) and application time (start ramp time, SRT) at 0.3333 pu/s and 0.02 s, respectively. Next, after the system stabilization the current was ramped-up to its final value (up-ramp final value, UFV) with an adjustable rate (up-ramp rate, UR) and execution time (up-ramp time, UT) at the final value of 1.0 pu, 9.0 pu/s and time of 0.3 s, respectively. Before stopping the converters (at stop time, ST) the current was ramped-down to the minimum current with an adjustable rate (down-ramp rate, DR) and execution time (down-ramp time, DT) at the value of -9.0 pu/s and at the time of 1.4 s, respectively. Finally, at stop time the reference was ramped-down to zero value at time of 1.6 s with the same rate used for the start ramp.

Fig. 5(a) and Table I show the firing delay angle (α_{ord}) control at this scenario. In this graphical result the α_{ord} for conventional controller (CVC) was added by 20° to differentiate the α_{ord} from the ANC result. It is shown that the α_{ord} was started at 90°. Next, the α_{ord} increased to 92° at time t_0 .

So, the α_{ord} decreased to 30° at time t_1 and decreased again to 26° until time 1.2 s. The α_{ord} increased to 40° at time t_2 , and increased again to 166° at time t_3 . Fig. 5(b) shows the mode operation of rectifier in this scenario. Firstly, the rectifier was operated in Blocked Mode from time 0.0 s until time t_0 , and the Blocked Mode operation was changed to Current Mode at time t_0 until 1.1 s. So, at time 1.1 s the rectifier was operated α_{min} Mode until time 1.25 s. Next, the rectifier was on Current Mode again until time t_3 and at time t_3 the rectifier operated was on Forced α Mode until t_4 . Finally, the rectifier was operated at Blocked Mode from time t_4 to infinite time.

Fig. 6(a) and Table II show that V_{dL} increased at the values from 0.05 to 1.06 pu at times from t_0 to t_1 , respectively. So, the V_{dL} decreased from 1.06 to 1.0 pu at times from t_1 to t_2 . Next, the V_{dL} decreased again from 1.0 to 0.96 pu at times from t_2 to t_3 , respectively. Finally, the V_{dL} decreased again from 0.96 to 0.25 pu at times from t_3 to t_4 . Fig. 6(b) shows DC line current (I_d) compared to reference current (I_{dref}). Firstly, at time t_0 the I_d was at the value of 0.04 pu until time t_1 . So, the I_d increased from 0.04 to 0.4 pu at time 4.0 s and increased again from 0.4 to 1.0 at time from 0.4 to 0.6 s. This I_d still at the value of 1.0 until t_2 . And, the I_d decreased from 1.0 to 0.0 pu at times from t_2 to t_3 .

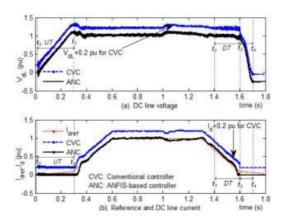


Fig. 6. The DC line voltage and current at normal operation.

Simulation shows that some results of proposed controller (ANC) in this scenario such as: Firing delay control, mode operation, voltage/current AC input and direct voltage/current output of rectifier are similar to the results of conventional controller (CVC). According to simulation results of the ANC, it is potential to replace the CVC by using ANC permanently. Moreover, to explore ability of the ANC on the HVDC at disturbances/faults condition that the topic will be explained in Scenario 2.

B. Performance of the Controller to cover disturbance/fault

Scenario 2: Four temporary disturbances/faults were forced to the HVDC system on different time. Location and time duration of the respective disturbance/fault are illustrated in Fig. 7. Control strategy of the rectifier to cover disturbance/fault is conducted by regulating the firing delay angle (α_{ord}) and by switching mode operation of this rectifier. Graphical visualization of the α_{ord} and mode operation are illustrated in Figs. 8(a) and (b), respectively. Firstly, positive pole to ground fault occurred at point F_1 of HVDC line from time 0.5 (t_{10}) to 0.6 s (t_{11}). The α_{ord} was regulated to the value of 16.5° at time t_{10} , and decreased to 16.2° from t_{11} until before t_{12} . Next disturbance, decreasing of reference current was occurred (F_2) at the value of -0.25 pu from time 0.75 t_{12} to 0.85 s (t_{13}).

In this condition, the α_{ord} increased sharply to 38.6° at time t_{12} , then at a moment it was decreased to 16.9° until time t_{13} . From time t_{13} to time a moment before 1.0 s (t_{14}) it was oscillated from 16.9° to 10.7°. Positive pole to ground fault occurred at point F_3 from time t_{14} to 1.1 s (t_{15}), the α_{ord} decreased to 8.0° at time t_{14} , the α_{ord} was increased to 11.0° at time t_{15} , then increased again to 12.0° before the time 1.2 s (t_{16}). Finally, three-phase fault to ground occurred at AC line₂ (F_4) from t_{16} to 1.3 s (t_{17}), the α_{ord} increased to 12.0° at time t_{16} , so the α_{ord} stayed at this value until time t_{17} . Completeness numerical result of the firing delay angle is listed in Table II.

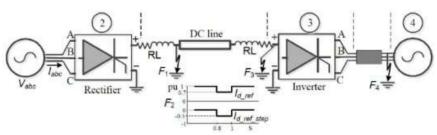


Fig. 7. The HVDC system is forced by disturbances/faults at F1, F2, F3 and F4 points.

From Fig. 8(b), it is shown that the rectifier was operated on α_{min} Mode at time from 0.0 s to 0.2499 s. From time 0.25 to 0.5299 s the rectifier operation was changed to Current Mode, then the rectifier operation was changed again to α_{min} Mode from time 0.53 to 0.5499 s. Next, from time 0.55 to 0.9099 the rectifier was on Current Mode, and it was in α_{min} or Mode Current alternately.

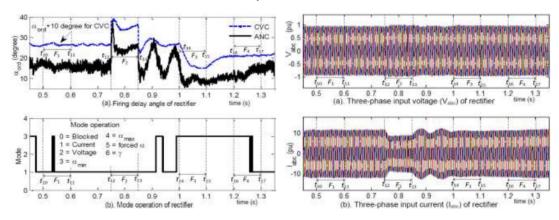


Fig. 8. Firing delay angle (αord) and mode operation of HVDC rectifier.

Fig. 9(a) shows the pattern of three-phase voltage input (V_{ph}) of rectifier. The voltage input varied from 0.99 to 0.92 pu for upper limit and lower limit, respectively. Dynamical of three-phase current input (I_L) is shown in Fig. 9(b) and listed in Table II. It is shown that the I_L was at the value of 11.3 pu at time t_{10} , this current increased to 11.89 pu at time t_{11} and increased again to 11.95 until time t_{12} . At time t_{12} , this current decreased from 11.95 to 9.01 pu at time t_{13} . At time t_{13} , this current oscillated in range of 11.0 - 11.20 pu until time t_{14} . From time t_{14} , t_{15} , t_{16} , and t_{17} this current increased from 11.10 to 11.20, 11.60, and 12.01 pu, respectively.

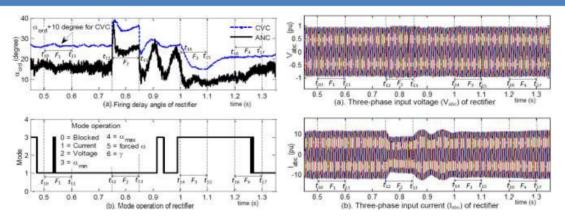


Fig. 9. Dynamical of AC input voltage and current.

Fig. 10(a) shows the pattern of DC line voltage (V_{dL}) for the conventional controller (CVC) and ANFIS-based controller (ANC). It is shown that the time at t_{10} , the V_{dL} was at the value of 1.0 pu, then this voltage decreased moderately to 0.99 and 0.98 pu at time t_{11} and until time t_{12} . At time t_{12} , this voltage decreased sharply to 0.822 pu, at a moment this voltage increased to 0.975 pu until time t_{13} . So, at time t_{13} this voltage increased sharply again to 1.15 pu and at a moment this voltage decreased and oscillated to 0.935 pu until t_{14} . At time t_{14} this voltage increased to 1.09 pu until time t_{15} , then this voltage decreased to 1.05 pu until time t_{16} . This voltage decreased again to 1.02 pu at time t_{16} and stayed in this voltage until t_{17} .

Dynamical of the reference current (I_{dref}), DC current (I_d) for the CVC and ANC are illustrated in Fig. 10(b). From Fig. 10(b) and Table II, it is shown that the I_d was at the value of 1.013 pu for time t_{10} , so the I_d decreased at a moment to 0.995 from time t_{11} to time t_{12} . Next, at time t_{12} the I_d decreased sharply to 0.775 pu, then it increased moderately to 0.780 until time t_{13} . At time t_{13} , the I_d increased and oscillated from 0.78 to 0.94 pu until time t_{14} , and at time t_{14} the I_d decreased to 0.77. Then, it increased to 0.945 and increased again to 0.948 pu for time t_{15} and time t_{16} , respectively. Finally, at the time t_{16} the I_d increased from 0.948 to 1.01 pu until time t_{17} . Simulation results in this scenario show that the DC currents produced by the CVC and ANC are able to follow the given reference current. The both controllers are working properly and they are giving good performances. Although, the I_d response of the ANC is still oscillate in severe disturbance case such as: When current reference is reduced to -0.25 pu (F_2). Some control strategies should be applied to improve the rectifier performance and to anticipate the I_d oscillation response when the rectifier is operated in severe disturbances/faults.

Table II Performance Of The Controller At Disturbances/Faults

Period (time) Observed value	(0.5 s)	(0.6 s)	(0.75 s)	(0.85 s)	(1.0 s)	(1.1 s)	(1.2 s)	(1.3 s)
α _{ord} (°)	16.5	16.5-16.2	16.2-38.6	38.6-16.9	16.9-8.0	8.0-11.0	11.0-12.0	12.0
$V_{ph(p-p)}(pa)$	0.965	0.965-0.945	0.93-0.99	0.99-0.92	0.96-0.98	0.975-0.968	0.968-0.961	0.056
$I_{L[p-p]}(pu/100MVA)$	11.3	11.89-11.95	11.95-9.01	9.01-11.10	11.10-11.20	11.20-11.60	11.60-12.01	12.01
V _{dL} (pu)	1.0	0.99-0.98	0.822-0.975	1.15-0.935	0.935-1.09	1.09-1.05	1.05-1.02	1.02
$I_d(pu)$	1.013	1.013-0.995	0.995-0.775	0.775-0.78	0.77-0.945	0.945-0.948	0.948-1.01	1.01
$P_d(pu)$	1.013	1.00287-0.7556	0.8179-0.7556	0.8913-0.7293	0.720-1.030	1.030-0.9954	0.9954-1.0302	1.0302

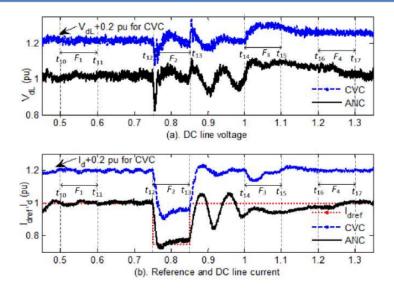


Fig. 10. Temporal of DC line voltage/current converter.

V. Conclusion

In this research ANFIS-based controller (ANC) is proposed to regulate the firing delay angle of 12-pulse rectifier HVDC. The ANFIS controller is implemented because computation complexity of the ANFIS controller is more efficient than that of fuzzy Mamdani controller. The ANC is built by training processes in off-line session with subtractive clustering method to generate membership function automatically. So, data training of the learning session are provided by simulating the HVDC with conventional controller in varied condition operations. During the learning processes, a 4000-point data set is used to learn the ANC controller per session. The structure of the ANC is built by five signal inputs (DC line voltage, DC current, reference current, block and forced α), and a firing delay angle signal as an output. The respective input of the ANFIS-based controller is represented by Gaussian membership function. Moreover, the output is described by linear membership function. Performance of the ANC is observed on the firing delay angle, mode operation, AC voltage/current input, DC line voltage, and DC current responses, respectively. Simulation results show that the

maximum power conversion is 1.0 pu at the firing delay angle 26°, the DC voltage and current are at the values of 1.0 pu when the HVDC operated in normal condition. Furthermore, the ANC is also able to cover temporary short circuit AC/DC fault on the HVDC. Meanwhile, the ANC responses are still oscillate when the reference current is reduced. Some efforts should be done to damp the oscillation in the next research.

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Chapter 7

Estimation of Ground Rod Depth for Effective Performance during Installation in Different Soil Types in Ibadan, South – West Nigeria

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Abstract. Poor or high resistance connection to the ground is one of the leading cause of earthing system failure. The resistivity of the soil and the depth to which an earthing electrode is driven directly affects the design and performance of a grounding system and it's a major factor that determines the Earth resistance of the grounding electrode. To achieve a reasonably low resistance connection to the ground, it is pertinent to carried out geophysical investigation to determine the variation of resistivity of layers below the surface and the earth resistance of the grounding rod prior to earthing system installation for optimization of rod driving depth. The survey areas cover Botany and Agricultural Departments University of Ibadan with coordinates N 7o 26' 58.4" E 3o 53' 47.9" and N 7o 26' 54.6", E 3o 53' 44.1" respectively and Nigeria Corporation Clay Mining Site, Omi Adio with coordinate N 7o 25' 48.1" E 3o 44' 47.2". A total of nine (9) Schlumberger Vertical Electrical Sounding (VES) (three VES for each location) was carried out using Geo pulse Tigre Resistivity meter. Earth resistance for grounding electrode was calculated for each geological layer of all the VES points within the survey sites, taking into account the resistivity and the depth of each lithological unit. The calculated results was compared with the standard (10 Ω) of a single rod to determine the depth of an earthing rod. Soil moisture content and particle size was carried out. The VES results showed that the second lithological layers of VES 1, 2, and 3 of Botany and Agricultural department of University of Ibadan had resistivity and depth ranged from 14.5 to 25.1 Ω m and 2.9 to 4.5 m; 19.8 to 53.1 Ω m and 5.6 to 9.8m respectively while the resistivity and depth of the second lithological layer for VES 1 and 2 of Omi Adio were 8.6 Ω m, 7.7 Ω m and 4.5 m, 6.9 m respectively and that of the third lithological layer was 11.5Ω m. Moisture contents results of Omi Adio, Agricultural and Botany Department ranged from 0.125 g/g to 0.35 g/g, 0.020 g/g to 0.0869 g/g and 0.0465 g/g to 0.117 g/g respectively The particle size analyses results revealed that the topsoil of Omi Adio, Botany and Agricultural Departments as Clay, Sandy loam and Sand respectively. The recommended depth of Omi Adio, Botany and Agricultural Departments ranged from 2.3 to 6.9m, 2.9 to 4.5m and 5.6 to 9.8m respectively.

Keywords: Earth resistance, earthing systems, geophysical investigation, vertical electrical sounding.

I. Introduction

Grounding is the control of abnormal voltages or currents through the proper application of Ohm's law (John Pfeifer, 2001). Grounding is the key to safety that is the protection of personnel from shock or electrocution, fire, protection of equipment and facility from failure, fire and protection of electrical circuit from cable failures, Proper grounding manifest when power system work fast enough to eliminate or at least minimize damage.

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