Simulation of ANFIS Controller to Line Commutation Based on Current Source Converter High Voltage Direct Current System

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***Abstract*—**Regulation of rectifier trigger angle is very important in high voltage direct current (HVDC) transmission system to maintain effectiveness of power delivery in the HVDC operation. To cover this regulation, adaptive neuro-fuzzy inference system (ANFIS) controller is proposed in this research to replace proportional integral (PI) controller. Before applied, the ANFIS controller is trained by data training that obtained from the PI controller in various scenario. The ANFIS controller performance is evaluated by assessing its percent error of direct current compared to current reference. The result shows that at start up scenario (up-ramp 6 pu/s), the percent errors of direct current are 4.47 and 4.61% for ANFIS and conventional controllers, respectively. Also, when the current reference is reduced, the percent errors of direct current are obtained at 2.37 and 2.51% for ANFIS and conventional controllers. The ANFIS controller is able to control the HVDC with percent errors of direct current are less than the percent errors of current for PI controller in two scenarios.

Keywords—ANFIS, control, HVDC, percent error, simulation

I. Introduction

The motivation of built direct current (DC) technology in transmission system is power efficiency. That losses transmission of power through DC system is less than the losses through AC system at the same power rating [1]. To coordinate the power transmission on high voltage direct current (HVDC) from sending-station to receiving-station as the consumer needed is the problem on operation of HVDC in power systems. This problem is studied by developing models in various methods such as: Thyristor-based current source converter (CSC)-HVDC system [2], converter controller and filter designs to increase load-ability of HVDC transmission system [3], small-signal dynamic and control of line-commutated-converter and voltage source converter HVDCs is built based on eigen-value analysis [4]. The modelling for LCC-HVDC is characterized by 4 models such as: Detailed electromagnetic transient simulation, transient stability, small stability and power flow models [5]. While, performance of HVDC system is discussed on steady state and under fault conditions [6].

To bridge power system and power semiconductor switching models, there are built average value model (AVM). The AVM is an effective method to implement switching dynamic model of converter where the high frequency of the converter is averaged and neglected [7]. It is more convenience to apply dynamic AVM for CIGRE first HVDC model in power system-level study than detailed switching-level model. The AVM is developed by some sets of nonlinear algebraic functions and solved by numerically computation [8].

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Interest of artificial intelligent (AI) application in power system is growth rapidly in recent years because the AI is attractive, interactive and easy to be implemented. The both fuzzy type-2 and ANFIS are applied in power stability of large power system [9], ANFIS is proposed to improve stability a three-bus power system [10], and the ANFIS method is used to control and to detect fault in HVDC system [11]. Continuous mixed p-norm fuzzy is developed to cover parameter uncertainties of onshore/offshore HVDC stations [12]. Fuzzy logic controller (FLC) shows better damped than PI control when applies in HVDC scale-model simulator [13]. The FLC application in power systems such as: to regulate interleaved DC-DC converter [14], to improve power quality, maintain power factor and reduce harmonic of distribution system [15], to control direct power for grid connected in distribution system [16], to drive permanent magnet synchronous motor [17] and to maintain of PV-wind hybrid system [18]. An adaline neural network (NN) is implemented to control HVDC links with feedback control. This NN control is able to stabilize operation of simplified HVDC model in normal and abnormal situations [19]. Improvement of multi-machine transient stability is done by NN control. Where, one of branch a 9-bus 3-machine is modified by HVDC line-network and controlled using NN algorithm [20]. ANFIS controllers are implemented to control of HVDC [21], HVDC light under AC fault [22] and inverter of HVDC in average value model [23]. However, the performance the ANFIS controller that applied to HVDC transmission has never been discussed before. This research proposes performance of ANFIS controller on rectifier-side of HVDC at start and when current reference is reduced.

This paper is organize as: Line commutated current source converter is described in Section II. Design of ANFIS controller is given in Section III. Simulation result and conclusion are given in Section IV and V, respectively.

II. Line-Commutation Based on Current Source Converter (CSC)

A. Thyristor-based CSC Mechanism

Thyristor is a solid-state switch that used in HVDC conversion mechanism. This device is available to cover the high-power turn-off switching processes. In this mechanism, the thyristor bridges are supposed ideal and connected to strongly AC system [1]. Basic principle for conducting sequence of simple three-phase rectifier is shown in Fig. 1. Where, thyristors 1, 3 and 5 at the top and thyristors 4, 6 and 2 at the bottom are connected to phases R (Red), Y (Yellow) and B (Blue), respectively. Fig. 1(a) shows current flows start from phase R through conducting valves 1 and 6, and the current flows to phase Y. Also, in Fig. 1(b), the current flows start from phase R through conducting valves 1 and 2, and the

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current flows to phase B. The mechanisms in Figs. 1(c), 1(d), 1(e) and 1(f) are similar to mechanism in Fig. 1(a). The complete switching mechanisms of rectifier are explained in [1].

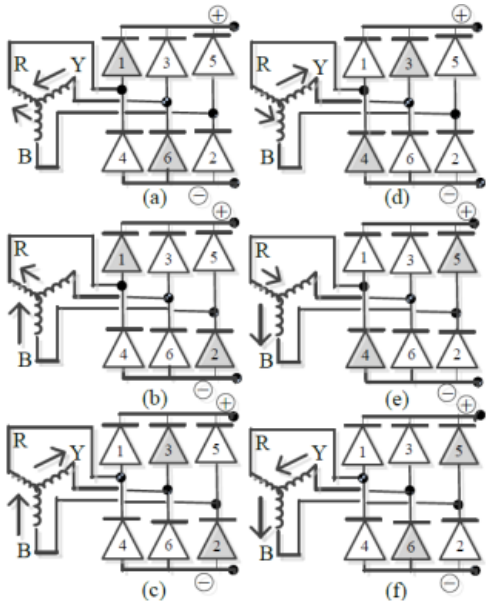

Fig. 1. Basic operation of three-phase rectifier.

B. Simple block diagram of CSC-HVDC system

Simple diagram block of current source converter-high voltage direct current (CSC-HVDC) is shown in Fig. 2(a). The CSC-HVDC diagram block in this paper is taken from [2], with some modifies to simplify the block. The block consists of 8 components: 1). Ideal 3-phase AC source at rectifier-side. 2). Rectifier converter. The function of rectifier converter is to convert the AC voltage/current into DC voltage/current. 3). High voltage DC transmission, where this transmission function is to transmit the DC voltage/current from sending-end to receiving-end. 4). Inverter converter at the receiving-end. The function of the inverter is to convert the DC voltage/current again into AC voltage/current. The AC voltage/current are distributed to consumers through step-down transformer. 5). Ideal 3-phase AC source at inverter-side. The ideal 3-phase AC source is operated as load of the HVDC system. 6). Master control. The function of master control is generated DC current reference I_{dref}. The DC current reference signal is to guide rectifier control with some commands such as: Start-up, up-ramp, down-ramp and stop-down. 7). Rectifier control. rectifier control function is to regulate trigger angle (*Alpha*). By guiding of the current reference, the DC voltage and current, the *Alpha* signal is produced in rectifier control. The *Alpha* is fed into 12-pulse firing control. 8). The 12-pulse firing control. Function of firing pulse is to provide trigger signal to fire the thyristor in the rectifier.

Fig. 2(b) shows dynamic signal of the DC current reference (I_{dref}). This signal was produced by the Master control and was fed into the converter rectifier controller. At start-up time at 0.02 s, the DC current reference was increased from 0.0 pu to 0.3 pu at time 0.32 s. From time 0.32 s to time 0.4 s, the value of the current was still at the value of 0.3 pu. Next, at time 0.4 s the current was increased to 1.0 pu at time 6.0 s with the value of up-ramp was at 6.0 pu/s. And, the final value was set at 1.0 pu until 1.6 s.

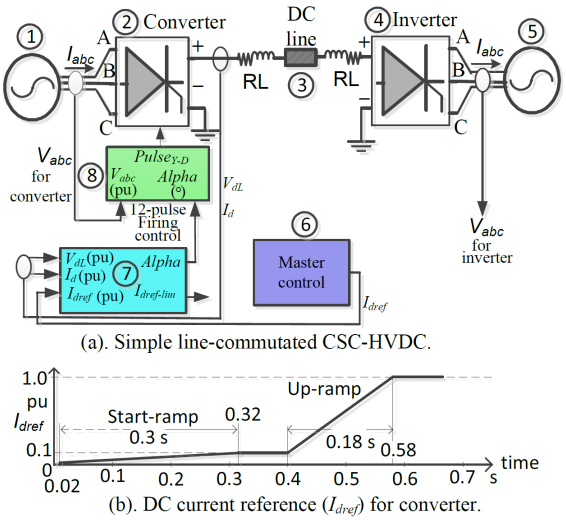

Fig. 2. HVDC block diagram and current reference at Master control.

C. Percent error of DC current

The performance of controller is measured by percent error of DC current. It is desirable to indicate the overall accuracy of final experiment by reporting some type of percent error in common experiment. When the quantity measured has a true value, then the experimental value accuracy is given by a ratio of the error to the true value [24]. Where, the percent error of DC current is obtained by comparing of the DC current (I_d) and DC current reference (I_{dref}). The percent error of DC current formula is written as:

$$Percent\ error = |(I_d - I_{dref})/\ I_{dref}\ | \times 100\ \% \qquad (1)$$

III. ANFIS Controller Design Process

Unit controller function is to control the level DC voltage/current in high voltage direct current (HVDC) system by regulating the trigger angle of the thyristor device [2]. Figs. 3(a) and (b) show the conventional and ANFIS controllers for CSC-HVDC system. Inputs of the rectifier controller block are DC voltage (V_{dL}), DC current (I_d), DC current reference (I_{dref}), Block and Forced alpha. The output signal of the controller is trigger angle (*Alpha*).

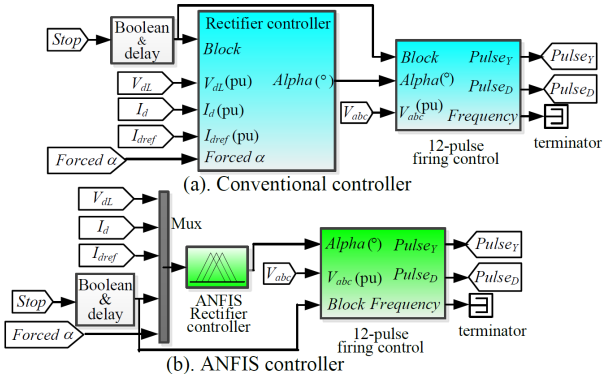

Fig. 3. Controller unit for CSC-HVDC system.

ANFIS controller is trained using input-output data set that obtained from simulating the CSC-HVDC equipped by conventional controller. In this training session, Sugeno-type fuzzy with subtractive clustering method was used to generate fuzzy inference system (FIS) function. Gaussian and linear functions were used for inputs and output membership functions, respectively. During update ANFIS parameters, back-propagation and least squares estimation methods were applied to optimize the parameters. After training session, four Gaussian membership functions were produced for DC current and DC current reference inputs as shown in Figs. 4(a) and (b), respectively. And, five linear membership functions (*outAlpha*1, *outAlpha*2, …, *outAlpha*5) were obtained for output membership function as shown in Fig. 4(c).

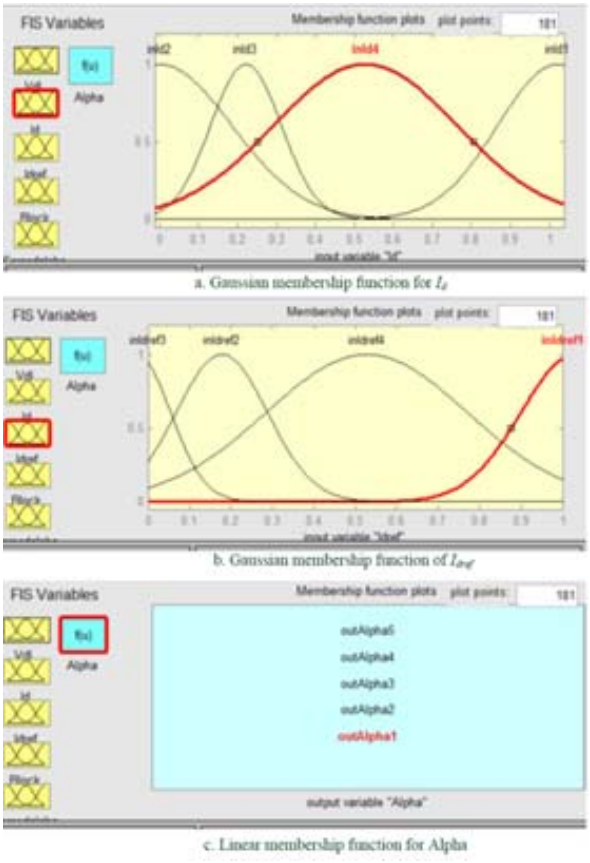

Fig. 4. Input-output membership function of ANFIS controller.

IV. Simulation Results

Program packaged Matlab/Simulink 7.9.0.529 (R2013b) [25] was used to simulate ANFIS controller. This program was run on Processor Intel core i5-700, 6.0 MB cache, 3.0 GHz, Motherboard LGA 1151 personal computer and Windows 7 operating system. Simulation results of the ANFIS controller are compared to results from conventional controller (proportional integral, PI) in order to validate the ANFIS controller simulation results. The simulations were done as follows.

A. Simulation at Start-up and Stop-down

In this paper, the ANFIS controller is used to control the rectifier block of HVDC system. Where, the PI controller that used as comparator for ANFIS controller was set at parameters proportional (P=2600); and integral (I = 26). The DC current reference (I_{dref}) was taken at master controller with parameter up-ramp/down-ramp at rates 4.0/–4.0; 6.0/–6.0 pu/s at time 0.3 s, and final value at 0.99 pu at starting time. Stop time was taken at 1.6 s and the simulation time was taken at time 1.8 s.

The simulation results for percent errors at start time (E_{STR}), steady state (E_{SS}), and stop time (E_{STP}) are listed in Table I. Also, simulation results for parameter up-ramp/ down-ramp at rate 6.0/−6.0 pu/s are shown in Figs. 5, 6 and 7 for (DC current and DC current reference), (DC voltage and trigger angle) and rectifier input currents, respectively.

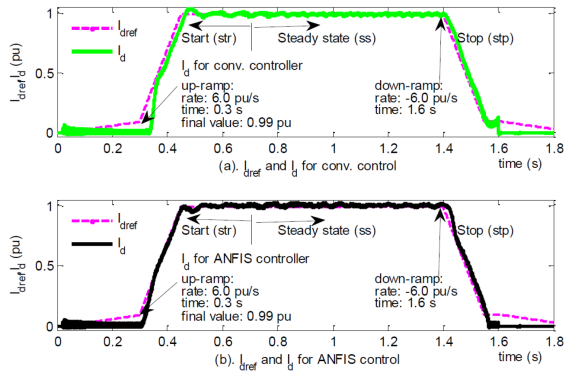

Fig. 5. Response of current reference and DC current.

From Table I, it is shown that percent error of current for ANFIS controller were obtained at the values of 4.21, 1.28×10^{-3} and 4.65% for start time (E_{STR}), steady state (E_{SS}), and stop time (E_{STP}), respectively, at up/down-ramp 4/–4 pu/s. The percent error of current for conventional controller were at 3.79, 3.57×10^{-3} and 4.72% for start time, steady state, and stop time, respectively. At up/down-ramp 6/–6 pu/s, these errors (ANFIS controller) were obtained at 4.47, 1.39 and 4.76% for start time, steady state, and stop time, respectively. And, percent error of current for conventional controller were obtained at 4.61, 4.03×10^{-3} and 4.85% for start time, steady state, and stop time, respectively. Based on the simulation results in Table I, it is shown that the percent error of current at steady state is smaller than the start time and stop time. All the percentage errors for ANFIS and conventional controllers are smaller than 5%, we call that the simulation results are valid.

TABLE I. Table Type Styles

up/ down ramp (pu/s)	ANFIS control			Conventional control		
	E_{STR} (%)	E_{SS} (%) $\times10^{-3}$	E_{STP} (%)	E_{STR} (%)	E_{SS} (%) $\times10^{-3}$	E_{STP} (%)
4;–4	4.21	1.28	4.65	3.79	3.57	4.72
6;–6	4.47	1.39	4.76	4.61	4.03	4.85

Figs. 5(a) and (b) show the DC current reference and DC current of conventional and ANFIS controllers for rectifier. It is shown that DC current (I_d) signals are able to follow the current reference (I_{dref}) signal with the percent error of respective controllers as listed in Table I.

Fig. 6(a) shows the direct current (DC) voltage (V_{dL}) for conventional and ANFIS controllers. At point a1, the DC voltage increased to point a2, with the maximum value at 1.2 pu. Next, this voltage decreased and oscillated, then achieved

steady state value at 0.99 pu at point a3 until before point a4 (1.4 s). At time (1.4 s) down-ramp of master control is ON position and this voltage was decreased to point a4, and decreased again at point to the zero value (0.0 pu) at point a6.

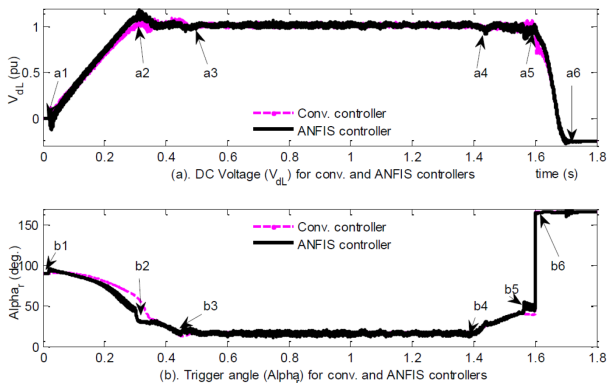

Fig. 6. Dynamic of DC volt. and trigger angle for start-up and stop-down.

Fig. 6(b) shows the trigger angle of rectifier thyristor (*Alpha*, °) for conventional and ANFIS controllers. At initial condition the trigger angle was set at 90°, from initial value the trigger angle increased to peak value at 110° (point b1), then decreased moderately to 22° at 3.8 s (for conventional controller). Trigger angle dynamic of ANFIS controller also decreased moderately at time of 3.5 s the value of 22° was achieved (at point b2). Next, the angles of both controllers are decreased to 17° at time 0.45 s (point b3) and these angles achieved steady state condition until before 1.4 s (point b4). At time 1.4 s (point b4) these angles increased to 22° until 1.56 s (point b5). At time 1.6 s these angles increased to 166° (point b6). At this condition, operation of rectifier is blocked and DC current (I_d) of rectifier is going to zero.

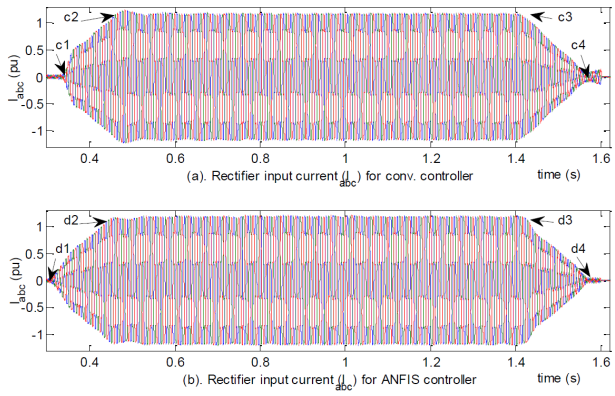

Fig. 7. Rectifier input currents I_{abc} for conv. and ANFIS controllers.

Fig. 7(a) shows the three phase input currents (I_{abc}) of rectifier for conventional controller. We can see that at time 0.35 s (point c1) the currents increased from 0.0 pu to 1.1/–1.1 pu max/min values at time 0.45 (point c2). The currents achieve steady state condition from time 0.45 (point c2) until before time 1.4 (point c3). Next, input currents decreased to zero from point c3 to point c4 at time 1.56 s. In Fig. 7(b) it is shown that these currents for ANFIS controller, at time 0.35 s (point d1) the currents increased from 0.0 pu to 1.1/–1.1 pu max/min values at time 0.45 (point d2). The currents achieve steady state condition from time 0.45 (point d2) until before time 1.4 (point d3). Next, these currents decreased to zero from point d3 to point d4 at time 1.56 s.

B. Simulation at DC Current Reference Reduced

In this scenario, the current reference (I_{dref}) value was reduced to 0.1 pu (from 0.99 to 0.89 pu) at time from 0.72 to 0.82 s. Simulation results are shown in Figs. 8, 9, 10, 11 and listed in Table II.

Fig. 8(a) shows dynamic of direct current (I_d) was compared to current reference for conventional controller. The current reference was set at up-ramp rate: 6.0 pu/s, time: 0.3 s and final value: 0.99 pu. The current reference increased at time 0.3 s from 0.1 pu to 0.99 pu at time 0.45 s. The direct current increased also from 0.1 pu (at time 0.37 s) and achieved final value (0.99 pu) at time 0.45 s. At time 0.72 until 0.82 s the reference current was reduced to 0.1 pu (0.99 to 0.89 pu). The direct current decreased and achieved value 0.89 pu at time 0.73 s, at time 0.82 s the direct current increased again to value 0.99 pu. Before the direct current achieved steady state at time 0.9 s, this current increased over the set point then decreased to steady state 0.99 pu. The reference was set to decrease to zero (down-ramp) to shut-down the rectifier. The down-ramp was set as follow: rate= –6 pu/s, time=1.4 s and stop time=1.6 s. The direct current decreased from value 0.99 pu (1.4 s) to zero at time 1.6 s.

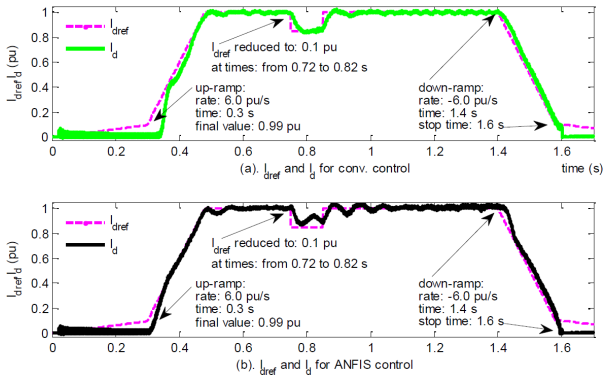

Fig. 8. DC current responses when current ref. (I_{dref}) reduced to 0.1 pu.

Fig. 8(b) shows the comparison of direct current and reference current of ANFIS controller. The setting values of reference current are same as in Fig. 8(a). The direct current increased gradually at time 0.3 s from value 0.1 to 0.99 pu at time 0.45 s. Then, this current slightly decreased and achieved steady state at time 0.5 s. At time 0.72 s as the reference current was reduced to 0.89 pu, the direct current decreased to 0.89 pu at time 0.79 s. Next, at time 0.82 s the direct current increased again toward 0.99 pu. In this state, the direct current oscillated slightly and achieved steady state at time 0.95 s. At time 1.4 s the direct current decreased to zero at time 1.6 s.

Table II shows percent error of current comparison for the conventional and ANFIS controllers. When the up-ramp/down-ramp: 4/–4 pu/s, it is shown that the percent error of current for the ANFIS and conventional controllers were obtained at the values of 2.18 and 2.26%, respectively. Next,

when the up-ramp/down-ramp were set at 6/–6 pu/s, the percent error of current for the ANFIS and conventional controllers were at the values of 2.37 and 2.51%, respectively. The ANFIS controller adequate to control the direct current of rectifier where the percent errors of current for this scenario (current reference reduced) are smaller than 5%.

Fig. 9(a) shows the DC voltage responses for conventional and ANFIS controllers when the current reference reduced from time 0.72 until time 0.82 s. At start-up time (point g1), the DC voltage increased from 0.0 pu to maximum voltages at the value of 1.2 pu (point g2). Next, this voltage decreased and achieved steady state at the value of 1,0 pu at time 4.9 s. At time 0.72 s when the current reference was reduced and at time 0.82 s when the current reference came-back to nominal value (1.0 pu), the DC voltage was oscillated as shown at points g3 and g4. The direct voltages achieved steady state until before time 1.4 s, at time 1.4 the voltages oscillated (point g5). Next, at time 1.6 s the voltages sharply decreased from 1.0 pu (point g6) to 0.0 pu at time 1.7 s (point g7).

TABLE II. PERCENT ERROR WHEN URRENT REFERENCE REDUCED

up/down ramp (pu/s)	ANFIS control	Conventional control
	Percent error (%)	*Percent error* (%)
4;–4	2.18	2.26
6;–6	2.37	2.51

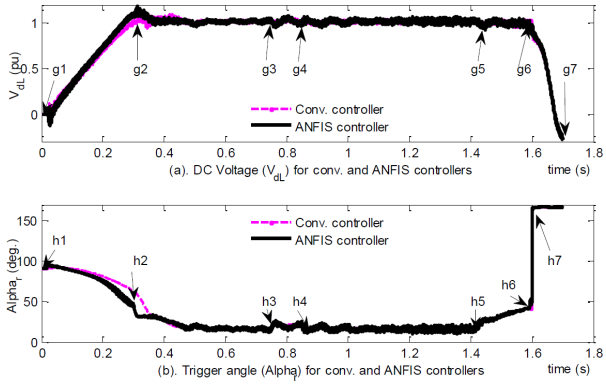

Fig. 9. Temporal responses of DC voltages and trigger angle (*Alpha*).

Fig. 9(b) shows the trigger angle (*Alpha*) for conventional and ANFIS controllers from when the current reference reduced from time 0.72 until time 0.82 s. At start-up, initial trigger angle was set at the values of 90° and these angles increased to 110° (point h1). Next, the angle gradually decreased to 22° at time 0.38 s for conventional controller. Meanwhile, the angle for ANFIS controller gradually decreased and achieved 22° at time 0.35 (point h2). The trigger angles of conventional and ANFIS controllers decreased again to 17° at time of 0.45 s and achieved steady state. At time 0.72 s the trigger angles increased to 18.5° (point h3), while at time 0.82 s these angles decreased again to 17° (point h4) and achieved steady state until time before 1.4 s. At time 1.4 s (point h5) the trigger angles increased moderately to 48° at time before 1.6 s. Finally, at time 1.6 s (point h6) the trigger angles jump to 166° (point h7) and the converter was stop to operate.

Fig. 10(a) shows the input currents (I_{abc}) of rectifier for conventional controller when the current reference was reduced at time 0.72 s until time 0.82 s. It is shown that at start time (from point i1 to point i2) the currents increased from 0.0 pu to 1.1/–1.1 pu max/min. Next, the currents decreased to 0.98/–0.98 pu max/min at time 0.72 s (point i3) until before time 0.82 s. At time 0.82 s the currents increased again to steady state condition at the values of 1.1/–1.1 pu max/min until before time 1.4 (point i4). Next, the input currents decreased to zero from point i4 to point i5 at time 1.56 s.

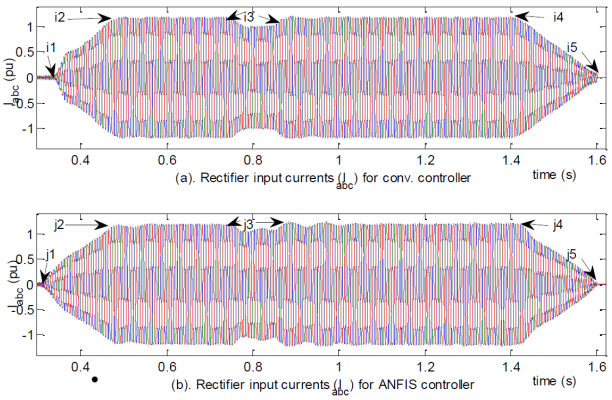

Fig. 10. Rectifier input currents (I_{abc}) when current reference reduced.

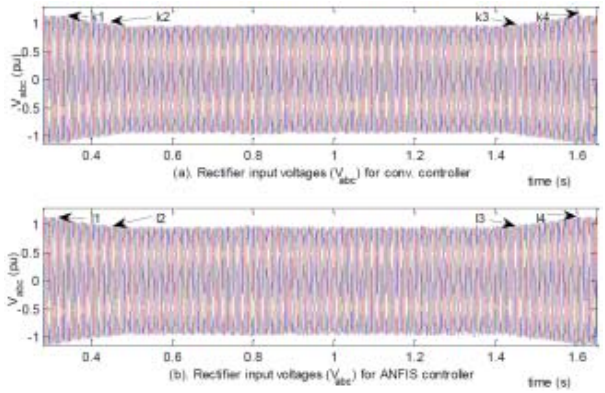

Fig. 11. Rectifier input voltages when current reference reduced.

The input currents of rectifier for ANFIS controller are shown in Fig. 10(b). At time 0.35 s (point j1) the currents increased from 0.0 pu to 1.1/–1.1 pu max/min values at time 0.45 (point j2). The currents achieved steady state condition at time 0.45 s. At time 0.72 s (point j3) the currents decreased to 0.98/–0.98 pu max/min until before time 0.82 s. At time 0.82 s, the currents increased to 1.1/–1.1 pu max/min values until before time 1.4 (point j4). Next, the input currents decreased to zero from point j4 to point j5 at time 1.56 s.

Input voltages of rectifier for conventional controller when the current reference reduced from time 0.72 s to time 0.82 s are shown in Fig. 11(a). The input voltages decreased from 1.1/–1.1 max/min pu values to the 1.0/–1.0 max/min values pu, from k1(at time 0.35 s) to k2 (at time 0.45 s). From 0.72 - 0.82 s, the increased of the voltages are not observed. The input voltages achieved steady state until time 1.4 s (point k3). Next, the input voltages increased again at time 1.4 s (point k3) - 1.6 s (point k4). Fig. 11(b) shows the input voltages decreased from 1.1/–1.1 pu (point l1) to 1.0/–1.0 pu (point l2) for the max/min values, from time 0.35 s to time 0.45 s. At the reduced current reference scenario, increased of the input voltages were very low and not observed. Steady state of the input voltages were achieved at 1.0/–1.0 pu for the max/min values until before time 1.4 s (point l3). Finally, at 1.4 s (point l3) the input voltages increased again to max/min values at 1.1/–1.1 pu at time 1.6 s (point l4).

Simulation results show that performance of ANFIS controller gives the percent errors are less than 5% for all scenarios. All these results are compared to the results from the conventional controller (PI) in order to validate the proposed controller. Some test scenarios such as: Three-phase fault, single fault-to-ground at AC-side, fault-to-ground at DC-side, current reference increased/decreased should be done to explore the potential application of the controller.

V. Conclusion

Power delivery control is the keyword to success in high voltage direct current (HVDC) system operation. To implement this control, ANFIS controller is proposed to regulate trigger angle of rectifier converter in the HVDC system. Performance of the controller is simulated on Start-up and DC current reference reduced scenarios. Results show at the up-ramp 4 and 6 pu/s, percent errors of current at start time are obtained at 4.21 and 4.47%, respectively, for ANFIS controller. At the same up-ramp value, percent errors of current at start time for conventional controller are at 3.79 and 4.61%. The effectiveness of the proposed controller is tested on reduced of DC current reference at time 0.72 to 0.82 s. When the up/down-ramp at 4/–4 and 6/–6 pu/s, the percent errors of current are obtained at 2.18 and 2.37% for ANFIS controller. At the same up/down-ramp parameters, the percent errors of current are obtained at 2.26 and 2.51% for conventional controller, respectively. In the future, applied of ANFIS controller in inverter-side is interest topic in this research field.

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