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Performance analysis of cascaded h-bridge multilevel inverter using mixed switching frequency with various dc-link voltages



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# Performance analysis of cascaded h-bridge multilevel inverter using mixed switching frequency with various dc-link voltages

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**Abstract.** Multilevel inverters have been widely used in many applications since the technology is advantageous to increase the converter capability as well as to improve the output voltage quality. According to the applied switching frequency, multilevel modulations can be subdivided into three classes, i.e: fundamental switching frequency, high switching frequency and mixed switching frequency. This paper investigates the performance of cascaded H-bridge (CHB) multilevel inverter that is modulated using mixed switching frequency (MSF) PWM with various dc-link voltage ratios. The simulation results show the nearly sinusoidal load output voltages are successfully achieved. It is revealed that there is improvement in output voltages quality in terms of THD and low-order harmonics content. The CHB inverter that is modulated using MSF PWM with equal dc-link voltage ratio (½ Vdc: ½ Vdc) produces output voltage with the lowest low-order harmonics (less than 1% of fundamental) while the CHB inverter that is modulated using MSF PWM with un-equal dc-link voltage ratio (2/3 Vdc: 1/3 Vdc) produces a 7-level output voltage with the lowest THD (16.31%) compared to the other PWM methods. Improvement of the output voltage quality here is also in line with improvement of the number of available levels provided in the output voltage. Here only 2 cells H-bridge inverter (contain 8 switches) are needed to produce a 7- level output voltage, while in the conventional CHB inverter at least 3 cells of H-bridge inverter (contain 12 switches) are needed to produce a 7-level output voltage. Hence it is valuable in term of saving number of component.

## 1. Introduction

Multilevel inverters have been widely used in many applications since the technology is advantageous to increase the converter capability as well as to improve the output voltage quality. Multilevel inverters are able to produce a staircase output waveform, that is more approaching sinusoidal and produce less number of harmonics compare to the conventional inverter output voltage. There are mainly three types of multi level inverters, Diode clamped, Flying capacitor inverter and cascaded h- bridge multi-level inverter [1].

Cascaded h-bridge multilevel inverters have been developed for utility applications including utility interface of renewable energy, voltage regulation, VAr compensation, and harmonic filtering in power systems. [1]. A modified cascaded H-bridge multilevel inverter (MLI) is implemented for solar applications [2]. A new design of asymmetric cascaded H-bridge multilevel inverter is implemented in the grid side of the wind energy conversion system [3]. A Five level cascaded H-bridge multilevel Inverter is also designed for induction motor drive [4].

There are three classes of switching frequency for multilevel modulations: fundamental, high, and mixed switching frequency. Fundamental Switching Frequency PWM (FSF PWM) methods produce switch commutations at output fundamental frequency and can be aimed to cancel some particular low frequency harmonic [5-6]. High Switching Frequency PWM (HSF PWM) methods are the adaptation of standard PWM to multi levels and they are meant to switch at very high frequency, about 10 to 20 kHz [7]. In this class there are Carrier-Based PWM (CB PWM) or Sinusoidal PWM, and Space Vector PWM (SV PWM). CB PWM is mainly divided into two categories: Level-Shifted (LS PWM) [8-9] and Phase- Shifted (PS PWM) methods [9]. Finally the LS PWM can be divided into Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD) modulations [10]. Mixed Switching Frequency PWM (MSF PWM) methods are those in which switches commutate at different frequency, like hybrid multilevel modulation, and are particularly suited for hybrid inverters where different cells can easily commutate at different frequencies [1].

A Hybrid / mixed PWM technique is a relatively new PWM strategy to control the CHB inverter. In the mixed switching frequency methods, one cell of H-bridge inverter is modulated in slow switching mode (fundamental frequency) and the other one is modulated in fast switching frequency mode, particularly using the level shifted carrier based PWM method and phase shifted carrier based PWM methods. The modulation technique offers possibility to apply various dc-link voltage ratios. This paper discusses the procedure to apply a mixed frequency PWM technique in the 2 cell CHB inverter with equal and un-equal dc link voltage ratios. The performance of cascaded 2-cell H-bridge (CHB) multilevel inverter using mixed switching frequency methods is investigated. The output voltages quality of the inverter in term of THD and the low order harmonics content are compared with the other PWM methods, namely fundamental frequency PWM, level shifted and phase shifted carrier based PWM methods.

## 2. Methodology

### *2.1 Cascaded h-bridge multilevel inverters*

The structure of the cascaded H-bridge (CHB) may consist of two or more H-bridge inverters. The CHB inverter can be supplied by separated DC sources or a single DC source. The structure of the CHB inverter with separated DC-sources is shown in Figure 1. This type of inverter consists of two cells H-bridge inverter hence employs 8 power electronic switches. The modulation technique that applies to each cell of inverter may be the same or different. It varies from fundamental switching frequency PWM, carrier based PWM or combination of the two different PWM methods (known as mixed / hybrid PWM method).

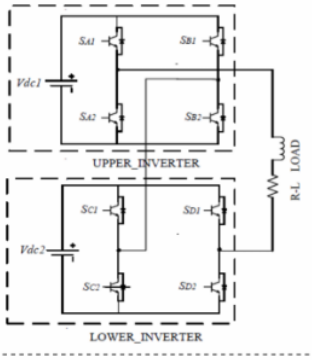


**Figure 1.** Five-level cascaded H-bridge inverter.

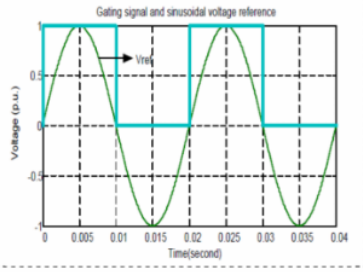


**Figure 2.** Gating signal using FSF PWM method

*2.2 Fundamental Switching Frequency (FSF)PWM*

Fundamental Switching Frequency PWM method controls the power electronic switches at fundamental frequency. The gating signals are simply generated by examining the sinusoidal voltage reference (Vref). When Vref has a positive (negative) value the upper (lower) switches are conducted (ON) otherwise the switches are dis-conducted (OFF).The operation of the FSF PWM method (for the upper switches) is governed using a simple logic as described in (1) and Figure 2.

$$\begin{aligned} if\ v_{ref} > 0\ then\ S_{(x=A,B,C,D)} &= 1\ (High) \\ else\ S_{x1(x=A,B,C,D)} &= 0\ (Low) \end{aligned} \tag{1}$$

Sx1 is the switching functions of the upper switches. The notation of switches refers to Figure 1. Since the switches operate in relatively slow switching, the output voltage contains high value of fundamental component as well as the low-order harmonics.

*2.3 Phase Shifted PWM (PS PWM)*

Phase Shifted PWM applies several triangular carriers that have the same frequency and same peak-peak amplitude, but there is a phase shift between any two adjacent carrier waves. For m voltage levels, (m-1) carrier signals are required and they are phase shifted with an angle of θ = (360°/m-1).

The gate signals are generated with proper comparison of carriers and a modulating signal. The comparison of voltage reference signal and triangular carriers and the respective gating signals for a five-level CHB inverter are shown in Figure 3 and 4.

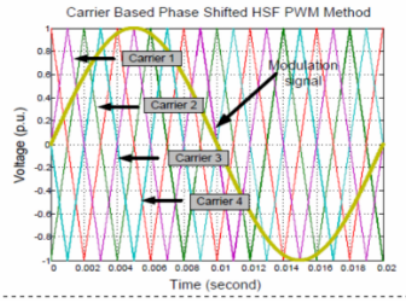


**Figure 3.** Comparison of modulation signal and carriers in PS PWM

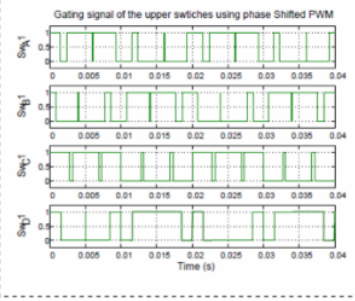


**Figure 4.** Gating signals using PS PWM of the CHB inverter upper switches

*2.4 Level shifted PWM (LS PWM)*

Level Shifted PWM also uses some carrier signals, but they are arranged in different levels among the carriers. According to the disposition of carrier waves, the LS PWM can be divided into three main types i.e (i) Phase disposition (PD), when all the carrier signals are in phase, (ii) Phase opposition disposition (POD), when all the carrier signals above zero reference are in phase but in opposition with those are below zero reference. (iii) Alternate phase opposition disposition (APOD): when the modulating signal of each phase is in opposition from each other.

The gating signals are generated by comparing the carrier waves and the modulating signal as shown in Figure 5 and 6.

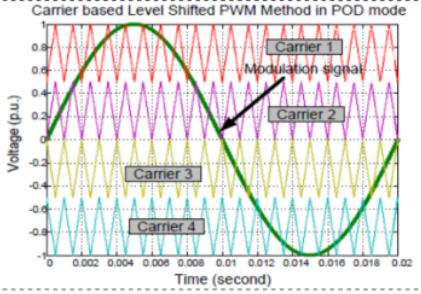


**Figure 5.** Comparison of modulation signal and carriers in LS PWM arranged in POD mode

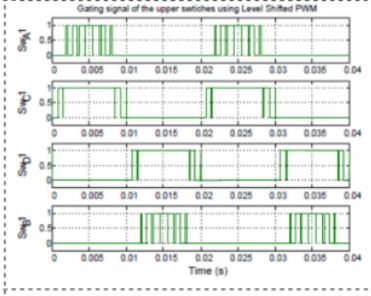


**Figure 6.** Gating signals using LS PWM for the CHB inverter upper switches

*2.5 Mixed Switching Frequency (MSF) PWM*

Mixed multilevel inverters may need different PWM strategies for the different stages composing them. For instance, a CHB inverter composed by one GTOs stage and one IGBTs stage may require two different switching frequencies, one for high-speed and one for low-speed devices. In this way, the output waveform, being the sum of the single stage outputs, presents the two frequencies in its harmonic content. The principle of a mixed switching frequency PWM of CHB inverter is shown in Figure 7.

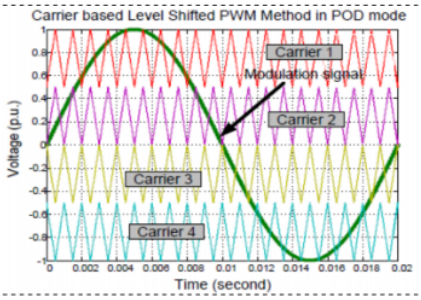


**Figure 7.** Schematic diagram of mixed switching frequency PWM of the CHB inverter

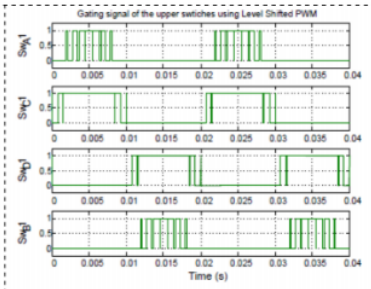


**Figure 8.** Method to generate the gating signals in MSF PWM (equal dc-link voltage)

The modulation signal of the MSF PWM is obtained by subtracting the sinusoidal reference signal and the output of the inverter that operates in FSF PWM. The gating signals for the inverter switches are generated by comparing the modulation signal and the triangular carriers. Figure 8 shows the modulation signal (bold line) along with the reference signal (dashed dot line) and output voltage of inverter operates in the FSF PWM (dashed line).

The gating signals of upper switches for the two H-bridge inverters are shown in the Figure 9. The gating signals of the lower switches are complementary to the gating signals of the upper switches. The gating signals of the MSF PWM with un-equal dc-link voltage ratio are generated in the same fashion as the equal dc-link voltage ratio.

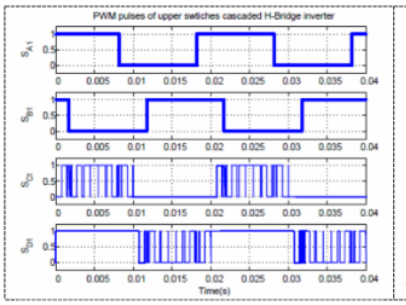


**Figure 9.** The gating signals of the CHB inverter with equal ratio of dc-link voltage

## 3. Simulations and Results

The developed PWM schemes were verified using computer simulations. The inverter is modelled using Sim-Power Blockset and the PWM pulses are generated using Simulink. In the simulation, the effect of inverter switches dead-times are neglected. Frequency switching of inverter operates in PWM mode is 1 kHz. The THD are calculated using (2) where the low order harmonics included in the calculation is up to 100.000 Hz (up to 2000th harmonics). The CHB inverter is supplied by separated dc-link voltages. Both inverters apply dc-link voltage ratio either 12 V : 12 V or 16 V : 8 V. In the two cases, the total of dc-link voltage is 24 V.

$$THD = \sqrt{\frac{\sum_{n=1,2,3,\ldots}^{r} V_n^2 - V_1^2}{V_1^2}} \quad (2)$$

Vn is the rms value of nth harmonic, V1 is the value of the fundamental component, n is the low-order harmonics and r is the maximum harmonic includes in the THD calculation.

### *3.1 Output voltage for DC-link ratio of ½ Vdc : ½ Vdc*

Figure 10 shows the output voltage of the multi-level CHB inverter using mixed switching frequency PWM technique with equal dc-link ratio and the respective harmonics spectrum. It is shown that the voltage output consist of 5 dc voltage levels {+24 V, +12 V, 0, -12 V, --24 V}. The fundamental component of the voltage output is 16.97 V (rms) and the value of THD is 25.39%. The harmonics spectrum indicates that the nearly sinusoidal waveform is achieved as the value of the low-order harmonics are significantly low. The zoom picture of the low order harmonics further shows the excellent quality of the output voltage. It reveals that the highest low order harmonics is the 15th harmonic (750 Hz) having the value of 2 V (rms) or 12% with respect to the fundamental, while the harmonics lower than the 13 harmonic are successfully eliminated by the proposed PWM method. All Switching combinations that produce 5 voltage levels in the output voltage are summarized in Table 1 [1].

Figure 11 and 12 show the output voltages of the individual inverter that are modulated using FSF PWM and HSF PWM methods and the respective harmonics spectrum. It is shown that the upper H-bridge inverter produces a three-level staircase waveform that contains high low-order harmonics and fundamental component. Meanwhile the lower H-bridge inverter also generates the same value of low-order harmonics. As a result the low-order harmonics do not appear in the output voltage. The lower inverter that operates in high switching mode has a role as a filter that prevents the low-order harmonics dismissed in the output voltage.

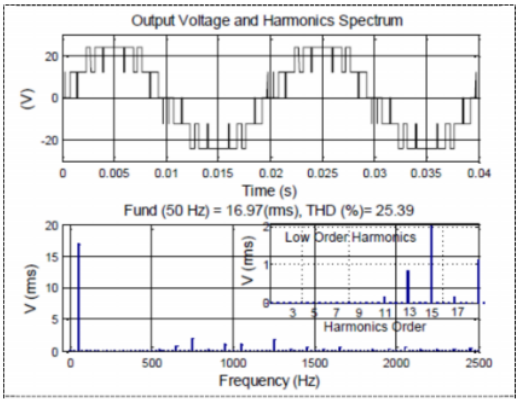


**Figure 10.** Output voltage and harmonics spectrum of MSF PWM method with dc-link ratio of ½ Vdc : ½ Vdc

**Table 1.** Operating switches with different voltage level for equal dc-link

| SWITCHES ACTIVATED | | | | | | | | VOLTAGE LEVEL |
|---|---|---|---|---|---|---|---|---|
| S A1 | S B1 | S C1 | S D1 | S A2 | S B2 | S C2 | S D2 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $24V\ (Vdc1+Vdc2)$ |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | $12\ V\ (Vdc2)$ |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $12\ V\ (Vdc1)$ |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | $12\ V\ (Vdc1)$ |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | $12\ V\ (Vdc2)$ |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | $-12\ V\ (Vdc1)$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | $-12\ V\ (Vdc2)$ |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | $-12\ V\ (Vdc1)$ |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $-12\ V\ (Vdc2)$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | $-24V\ (-Vdc1-Vdc2)$ |

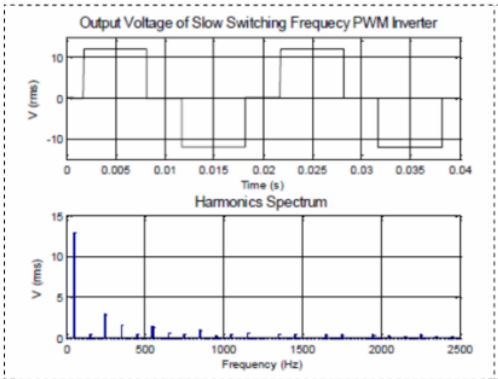


**Figure 11.** Output voltage of the FSF modulated inverter and harmonics spectrum

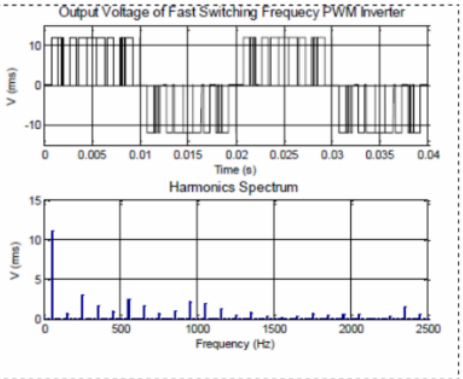


**Figure 12.** Output voltage of the HSF modulated inverter and harmonics spectrum

*3.2 Output voltage for DC-link ratio of 1/3 Vdc: 2/3 Vdc*

Figure 13 shows the output voltage of the multi-level CHB inverter using mixed switching frequency PWM technique with un-equal dc-link ratio of 2/3 Vdc :1/3 Vdc. It is clearly shown that the voltage output consist of 7 dc voltage levels {+24V, +16 V, +8 V, 0, -8 V, -16 V, -24 V}. The fundamental component is 16.97 V (rms) and the value of THD further improved to 16.41%. The zoom picture of the harmonics spectrum shows that the low-order harmonics are successfully suppressed into less than 5 % with respect to fundamental hence the output voltage is considered very close to sinusoidal. The improvement of the output voltage quality relates to the increased number of levels. This is the significant merit of the proposed PWM method. In the conventional CHB inverter, 3 cells H-bridge inverter (contains of 12 switches) are required to achieve seven levels in the output voltage. The number of level (l) is governed by, (l = 2n +1), where n is number of cell of H-bridge inverter [1]. In this method, only 2 cells H-bridge inverter (contains of 8 switches) are utilized to get a seven-level output voltage. All switching combinations that produce 7 voltage levels in the output voltage are summarized in Table 2 [1].

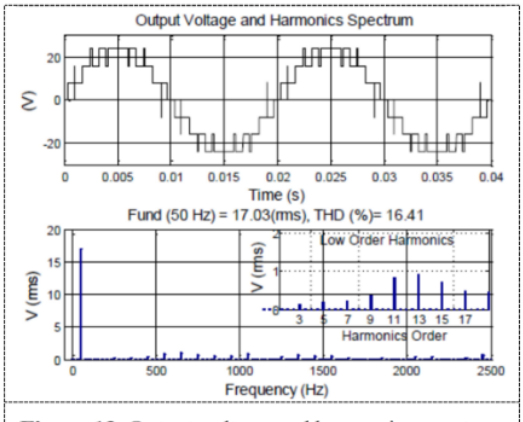


**Figure 13.** Output voltage and harmonics spectrum of MSF PWM method with dc-link ratio of 2/3 Vdc : 1/3 Vdc

**Table 2.** Operating Switches with different voltage level for unequal dc-link

| SWITCHES ACTIVATED | | | | | | | | VOLTAGE LEVEL |
|---|---|---|---|---|---|---|---|---|
| S A1 | S B1 | S C1 | S D1 | S A2 | S B2 | S C2 | S D2 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $24V(Vdc1+Vdc2)$ |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | $8\ V\ (Vdc2)$ |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $16\ V\ (Vdc1)$ |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | $16\ V\ (Vdc1)$ |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | $8\ V\ (Vdc2)$ |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | $-16\ V\ (Vdc1)$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | $-8\ V\ (Vdc2)$ |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | $-16\ V\ (Vdc1)$ |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $-8\ V\ (Vdc2)$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | $-24V\ (-Vdc1-Vdc2)$ |

The output voltages of the individual H-bridge inverters are shown in Figure 14 and 15. It is further confirmed that both inverters produce the respective low-order harmonics with almost the same magnitude hence avoid them to appear in the output voltage. In the ratio of 2/3 Vdc: 1/3 Vdc, the upper inverter generates relatively higher value of fundamental than the lower inverter. This implies that the upper inverter supplies more power to the load than the lower inverter. The benefit of this is that different power electronics switches may be used between two inverters. Yet the extra precaution should be taken to avoid the power transferred from upper inverter to lower inverter.

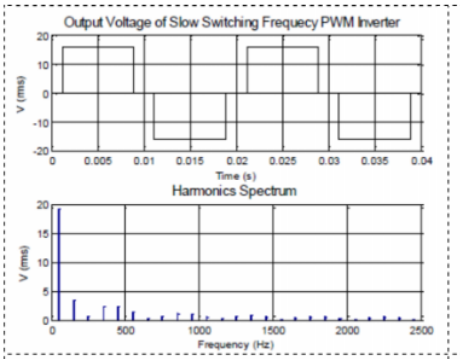


**Figure 14.** Output voltage of the FSF modulated inverter and harmonics spectrum

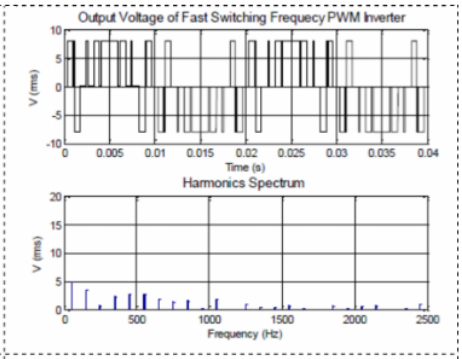


**Figure 15.** Output voltage of the HSF modulated inverter and harmonics spectrum

In order to further reveal the performance of the proposed PWM schemes, the THD and the content of the low-order harmonics is noted and compared with numerous PWM methods as presented in Figure 16. It is shown that the mixed frequency PWM with equal dc-link voltage (Mixed PWM-1) presents The lowest low-order harmonics among the other PWM methods while the mixed frequency PWM with un-equal dc-link voltage (Mixed PWM-2) shows the lowest THD (16.31%) among the other PWM methods.

Further investigation also found that the magnitude and position of the carrier signals in the mixed frequency PWM does not influence the quality of the output voltages. However, when phase shifted PWM method is applied in the mixed switching frequency PWM method, it is important to note that (based on the simulation process) the frequency switching have to be proportionally reduced twice as the frequency switching of the level shifted PWM in order to achieve a fair comparison.

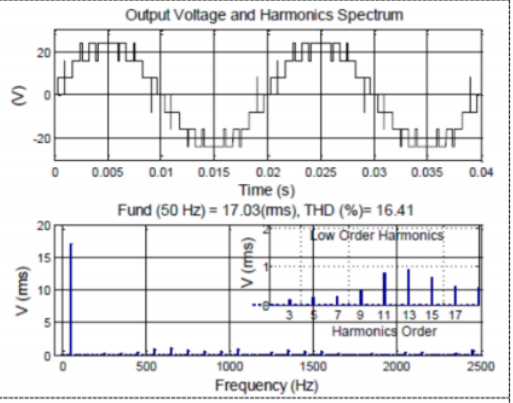


**Figure 16.** Comparison of low-order harmonics and THD of various PWM methods in CHB inverter

## 4. Conclusion

This paper investigates the performance of 2-cells CHB multilevel inverter that is operated in mixed switching frequency method with various dc-link voltage ratios. The developed PWM schemes produce output voltage with improved quality. The MSF PWM with equal dc-link produces output voltage with significant low low-order harmonics content (less than 1 % of fundamental) while the MSF PWM with un-equal dc-link voltage produces 7-levels in the output voltage in line with the lowest THD (16.31%) among several other PWM methods. Improvement of the voltage output quality is in line with number of available levels in the output voltage. Here only 2 cells H-bridge inverter (contain 8 switches) are needed to produce a 7-level output voltage, while in the conventional CHB inverter at least 3 cells of H-bridge inverter (contain 12 switches) are needed to produce a 7-level output voltage. Hence it is valuable in term of saving number of component.

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GENERAL COMMENTS

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