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Message from The Organizing Committees

Welcome to

The 36th Annual Conference of the IEEE Industrial Electronics Society
4th IEEE International Conference on E-Learning in Industrial Electronics
2010 IES Industry Forum

Renaissance Hotel & Conference Center, Glendale, AZ, USA

November 7 – 10, 2010

We are delighted to jointly host three events this year:

- IECON – the flagship annual conference of the Industrial Electronics Society
- ICELIE – the discussion of modern education and electronic learning methods for teaching in the field of industrial electronics
- IES Industry Forum – an opportunity to focus on industry directions and the use of emerging technologies in industry products

It is a blessing that the preparation for all events has developed smoothly – thank you for your help and participation.

Over 113 technical sessions have been organized to share technological advances, educational methods, and industry interests related to:

- Power Electronics & Renewable Energy
- Electrical Machines & Drives
- Control Systems & Applications,
- Sensors, Actuators and Systems Integration
- Signal and Image Processing & Computational Intelligence
- Mechatronics & Robotics
- Factory Automation & Industrial Informatics.

Nearly 50 sessions have special focuses, and there are nine tutorials covering a broad spectrum of IES technical interests.

Approximately 850 manuscripts were submitted to either IECON or ICELIE, of which 555 appear among the two combined final programs. Just over 1,000 reviewers participated in the technical review processes. On average, each paper received 2.96 peer reviews, followed by another final review from the respective program committees.

Other technical program highlights include:

1. Three plenary presentations that challenge the frontiers of industrial electronics:

   (a) *Manufacturing complexities with advanced silicon technologies* (Monday)

   Mr. Joshua M. Walden, Vice President of the Technology and Manufacturing Group and General Manager of Fab/Sort Manufacturing, Intel Corporation

   (b) *Advances of future vehicles and social adaptation* (Tuesday)

   Tadao Saito, Chief Technical Officer of Toyota-InfoTechnology and Professor Emeritus, The University of Tokyo

   (c) *Electrotextiles: Challenges and opportunities* (Wednesday)

   Alex Q. Huang, Professor and Director of the NSF FREEDM Systems Center, North Carolina State University.

   The keynote presentations will commence immediately after the morning technical sessions, to be followed immediately by a light lunch.

2. Industry Keynote Presentation (Tuesday during lunch): *From Companion Chips to Complete Solution*

   Arun Iyengar, Sr. Director, Military, Industrial, and Computer Division, Altera Corporation

3. The IES Industry Forum (Tuesday): This forum has over 14 industry speakers divided across four sessions: the Connected Vehicle, the Electrical Vehicle, Manufacturing, and FPGA and Silicon. In addition, Altera is sponsoring two raffles for Industry Forum attendees.

Conference attendees are invited to mingle at a variety of social events, including the welcome reception (Monday evening), conference banquet (Tuesday evening), light lunches (daily), and coffee breaks (morning and afternoon). Authors breakfasts are also provided Monday through Wednesday.

In addition to the onsite programs, we encourage you to enjoy a variety of outstanding local attractions in and around Phoenix, AZ. The IEEE Phoenix Section has prepared a menu of wonderful events.

We would like to thank all conference committee members and colleagues who have graciously volunteered their time and efforts for these events. We sincerely appreciate our sponsors, including Intel and Altera, for their financial support for IECON10. Thanks also go to our technical sponsors: New Jersey Institute of Technology, North Carolina State University, Auburn University, The Society of Instrument and Control Engineers (SICE) of Japan, and the IEEE Phoenix Section. Logistical support from IEEE Conference Management Services is gratefully acknowledged.

Sincerely,

The Organizing Committees of IECON10, ICELIE10, and the 2010 IES Industry Forum

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A five-phase multilevel space-vector PWM algorithm for a dual-inverter supplied drive(Conference Paper)

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Abstract

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Indexed keywords

Engineering uncontrolled terms: Balancing algorithms; Five-Phase Inverters; Five-phase machines; Harmonic performance; Hybrid powertrain; Low order harmonics; Multilevel converter; Open-end windings; Output phase; Output voltages; Phase spaces; Propulsion motors; Space vector PWM; Vector modulators

Engineering controlled terms: Algorithms; Electric inverters; Electric machinery; Electric windings; Harmonic analysis; Industrial electronics; Phase space methods; Variable speed drives; Winding

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A Five-Phase Multilevel Space-Vector PWM Algorithm for a Dual-Inverter Supplied Drive

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***Abstract*–Open-end winding variable speed drives with dual-inverter supply have been extensively investigated for various applications, including series hybrid powertrains and propulsion motors. The topology is simple to realise while offering a higher number of switching states without the need for capacitor balancing algorithms, when compared to standard multilevel converters. The existing body of work is however restricted to the three-phase electric machinery. This paper looks at the possibility of using a five-phase machine in an open-end winding configuration with dual five-phase inverter supply for these applications. Two possible space-vector PWM (SVM) algorithms are developed in the paper. The SVM schemes are relatively simple and use two two-level five-phase space-vector modulators, which have been previously shown to generate output voltages with minimum low-order harmonic content. The first SVM method has identical performance to the standard two-level inverter since it develops nine-level output phase voltage. The second method generates up to seventeen-level output phase voltage and therefore offers superior harmonic performance. The developed schemes are verified via simulation and the harmonic performance is analysed.**

I. INTRODUCTION

The concept of cascading two voltage source inverters (VSIs), one at each side of an open-end stator winding, was originally proposed in [1,2]. Typically, two two-level three-phase VSIs are utilised. Application of such a dual-inverter supply enables drive operation with voltage waveform equivalent to the one obtainable with a three-level VSI in single-sided supply mode. Three-phase open-end winding dual-inverter fed drive systems are currently considered as possible alternative supply solutions in EVs/HEVs [3-6], for electric ship propulsion [7], rolling mills [8], etc.

In applications such as EVs, where dc bus voltage is rather low and limited, the main reported advantage with respect to the equivalent multilevel single-sided supply is that a machine with a lower current rating can be utilised since the voltage across phases can be higher when two independent batteries are used instead of a single one [3,6]. Assuming that both inverters are two-level, the number of the switches is the same as in the equivalent three-level single-sided supply. However, additional diodes used in the diode-clamped (NPC) VSI are not needed, leading to a saving in the overall number of components. The problem of capacitor voltage balancing does not exist if the supply is two-level at each winding side.

The two VSIs, applied at the two sides of the three-phase open-end winding, can be of the same or of a different number of levels, with application of the two two-level VSIs being the most commonly analysed case. Analyses of the system with two three-level inverters are reported in [1,7,9], while use of a combination of a two-level and a three-level VSI has been considered in [8]. Topologies based on the inverters with higher number of levels have also been investigated, e.g. [10].

Multi-phase (more than three stator phases) variable-speed drive and generation systems are currently regarded as another type of potentially viable solutions for the same applications, including EVs/HEVs [11]. A two-level multi-phase VSI is the standard solution, with the star-connected machine winding and an isolated neutral point. Since multilevel and multi-phase topologies share a number of common features, it appears to be logical to try to combine them by realising multilevel multi-phase drive architectures. Yet, such attempts are rather rare, with very few examples [12,13], all related to the single-sided supply mode.

The only known example where a multi-phase drive system in an open-end winding configuration has been considered is [14]. An asymmetrical six-phase induction motor drive, with supply provided from both ends by means of two two-level six-phase VSIs (each composed of two three-phase VSI units) has been analysed. Two isolated dc voltage supplies are used as the inverter inputs at two winding ends. The goal in [14] was in essence low-order harmonic elimination/reduction rather than the multilevel operation. As a consequence, multilevel operation is neither attempted nor achieved and the drive is operated in all regimes with the voltage waveform equivalent to two-level VSI supply in single-sided mode.

On the basis of the provided survey, it follows that PWM algorithm for multilevel five-phase supply in open-end winding configuration has never been either addressed or realised. This paper therefore represents the first attempt in this direction. General properties of the five-phase ac motor drives with sinusoidal winding distribution are at first reviewed, along with the previously developed two-level SVM algorithm for a five-phase two-level VSI [15-17], which uses two large and two medium active space vectors per switching period in order to minimise low-order harmonics. Next, mathematical model of the cascaded topology is given, along with mapping of the space vectors that are of interest into the torque-producing 2D sub-space. Two simple SVM schemes are further developed, based on the two-level SVM algorithm for a five-phase VSI in single-sided supply mode. The performance of the SVM methods is investigated and verified via simulation for a range of modulation index values in the linear operating region and the resulting harmonic performances are discussed.

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II. PRELIMINARY CONSIDERATIONS

Prior to considering the SVM schemes for the open-end winding topology, it is beneficial to review the basic relationships which govern the performance of five-phase drives and the corresponding two-level SVM technique for a five-phase VSI. A five-phase machine can be modelled in two 2D sub-spaces, so-called α-β and x-y sub-spaces [11]. It can be shown that only current harmonic components which map into the α-β sub-space develop useful torque and torque ripple, whereas those that map into the x-y sub-space do not contribute to the torque at all. A multi-phase machine with near-sinusoidal magneto-motive force distribution presents extremely low impedance to all non-flux/torque producing supply harmonics and it is therefore mandatory that the supply does not generate such harmonics. What this means is that the design of a five-phase PWM strategy must consider simultaneously both 2D sub-spaces, where the reference voltage, assuming pure sinusoidal references, is in the first plane while reference in the other plane is zero. Two-level five-phase inverters can generate up to 2^5=32 voltage space vectors with corresponding components in the α-β and x-y sub-spaces, as shown in Fig. 1. Space vectors are labeled with decimal numbers, which, when converted into binary, reveal the values of the switching functions of each of the inverter legs. Active (non-zero) space vectors belong to three groups in accordance with their magnitudes - small, medium and large space vector groups. The magnitudes are identified with indices s, m, and l and are given as $|\bar{v}_s| = 4/5\cos(2\pi/5)V_{dc}$, $|\bar{v}_m| = 2/5\,V_{dc}$, and $|\bar{v}_l| = 4/5\cos(\pi/5)V_{dc}$, respectively. Four active space vectors are required to generate sinusoidal voltages [15-16]. Suppose that the reference space vector in the α-β plane is in sector $s = 1$ (Fig. 2a). Two neighbouring large and two medium space vectors are selected. In order to provide zero average voltage in the x-y plane (Fig. 2b) times of application of active space vectors become [15-16]:

$$t_{al} = \frac{2\sin(2\pi/5)}{V_{dc}}\sin(s\,\pi/5 - \vartheta)|\bar{v}^*|\,t_s$$
$$t_{am} = \frac{2\sin(\pi/5)}{V_{dc}}\sin(s\,\pi/5 - \vartheta)|\bar{v}^*|\,t_s \quad (1)$$

$$t_{bl} = \frac{2\sin(2\pi/5)}{V_{dc}}\sin[\vartheta - (s-1)\,\pi/5]\,|\bar{v}^*|\,t_s$$
$$t_{bm} = \frac{2\sin(\pi/5)}{V_{dc}}\sin[\vartheta - (s-1)\,\pi/5]\,|\bar{v}^*|\,t_s \quad (2)$$

where t_s is the switching period, ϑ is the reference position and indices a and b are defined in Fig. 2a. Total time of application of zero space vectors $t_o = t_s - (t_{al} + t_{am} + t_{bl} + t_{bm})$ is equally shared between zero space vectors $\bar{v}_0$ and $\bar{v}_{31}$. The maximum peak value of the output fundamental phase-to-neutral voltage in the linear modulation region is $v_{\max} = V_{dc}/[2\cos(\pi/10)] = 0.525V_{dc}$ [17]. Switching pattern is a symmetrical PWM with two commutations per each inverter leg. To demonstrate the validity of the technique and provide a benchmark for comparison purposes, simulations

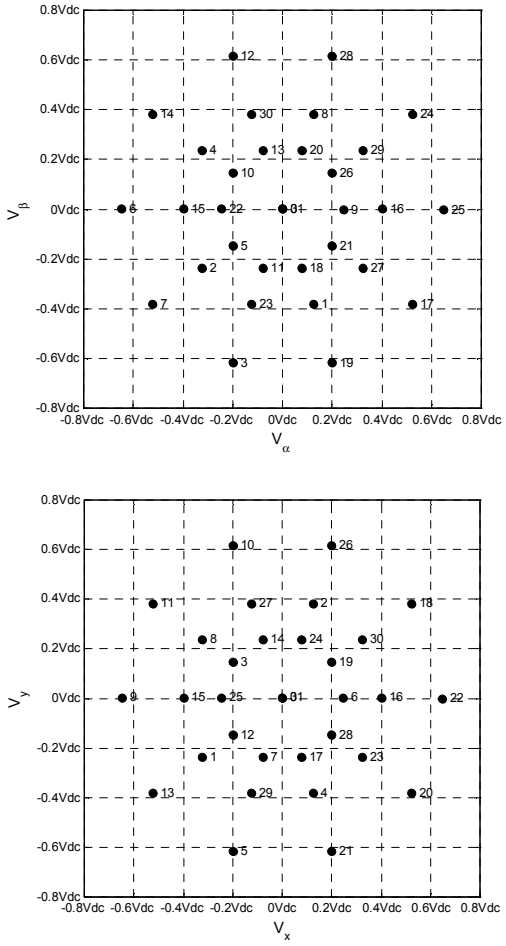

Fig. 1. Two-level five-phase VSI space vectors in the α–β and x-y planes.

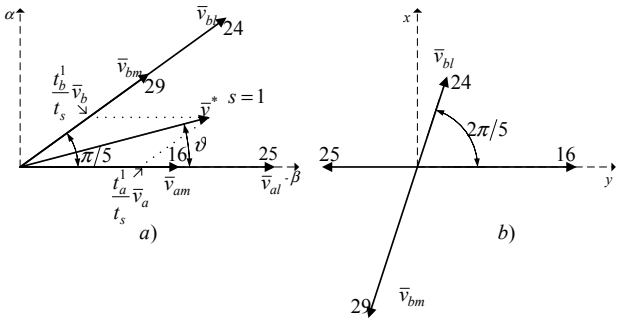

Fig. 2. Principle of calculation of times of application of the active space vectors (vectors are shown in the α–β (a) and x-y (b) planes and the reference in the x-y plane equals zero).

are performed for two settings of the modulation index $M = |\bar{v}^*|/(0.5V_{dc})$. Dc link voltage is set to 600 V, reference frequency is 50 Hz and the switching frequency of the VSI is 1 kHz. The results are illustrated in Fig. 3.

It can be seen from Fig. 3 that the output phase voltage waveform comprises nine levels and practically does not contain any low-order harmonics when the VSI is operating in the linear region with either a low value of the modulation index (0.1) or at the upper limit (1.05).

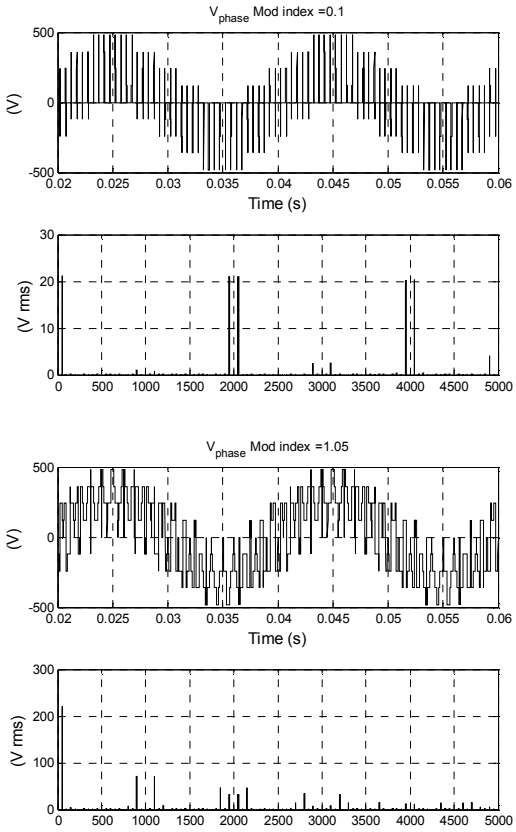

Fig. 3. Two-level five-phase VSI SVM: phase voltage waveforms and spectra for $M = 0.1$ and $M = 1.05$.

III. Five-Phase Open-End Winding Topology

Fig. 4 illustrates the open-end winding structure, based on utilisation of two two-level five-phase VSIs. The two inverters are identified with indices 1 and 2. Inverter legs are denoted with capital letters, *A,B,C,D,E* and the negative rails of the two dc links are identified as *N*1 and *N*2. Machine phases are labelled as *a,b,c,d,e*. Phase voltage positive direction is with reference to the left inverter (inverter 1). Using the notation of Fig. 4, phase voltages of the stator winding can be given as:

$$\begin{aligned} v_a &= v_{A1N1} + v_{N1N2} - v_{A2N2} \\ v_b &= v_{B1N1} + v_{N1N2} - v_{B2N2} \\ v_c &= v_{C1N1} + v_{N1N2} - v_{C2N2} \\ v_d &= v_{D1N1} + v_{N1N2} - v_{D2N2} \\ v_e &= v_{E1N1} + v_{N1N2} - v_{E2N2} \end{aligned} \tag{3}$$

Two isolated dc supplies are assumed so that the common mode voltage (CMV) v_{N1N2} is of non-zero value (the issue of CMV elimination is not addressed here). The resulting space vectors in dual-inverter supply mode will depend on the ratio of the two dc bus voltages. The situation considered further on is the setting $V_{dc1} = V_{dc2} = V_{dc}/2$, which gives the equivalent of single-sided three-level supply. Here V_{dc} stands for the equivalent dc voltage in single-sided supply mode. Since in five-phase case single-sided supply gives nine levels

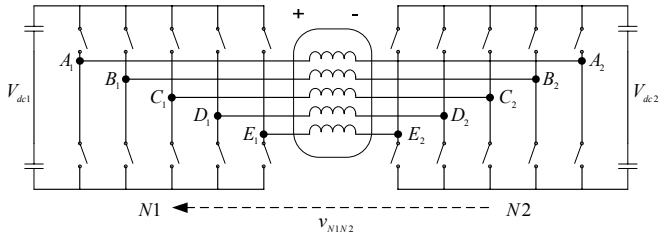

Fig. 4. Five-phase machine with dual two-level inverter supply.

in the phase voltages, it is expected that in five-phase case with dual-inverter supply there will be up to 17 levels in the phase voltage. The increased number of phase voltage levels is a consequence of the much greater number of switching states and voltage space vectors, generated by the converter, when compared to the single-sided supply mode.

Space vectors of phase voltages in the two planes are determined with

$$\begin{aligned} \bar{v}_{\alpha-\beta} &= (2/5)\left(v_a + \underline{a}v_b + \underline{a}^2 v_c + \underline{a}^3 v_d + \underline{a}^4 v_e\right) \\ \bar{v}_{x-y} &= (2/5)\left(v_a + \underline{a}^2 v_b + \underline{a}^4 v_c + \underline{a}^6 v_d + \underline{a}^8 v_e\right) \end{aligned} \tag{4}$$

where $\underline{a} = \exp(j2\pi/5)$. Using (3) and (4), one gets

$$\begin{aligned} \bar{v}_{\alpha-\beta} &= \bar{v}_{\alpha-\beta(A1B1C1D1E1)} - \bar{v}_{\alpha-\beta(A2B2C2D2E2)} \\ \bar{v}_{x-y} &= \bar{v}_{x-y(A1B1C1D1E1)} - \bar{v}_{x-y(A2B2C2D2E2)} \end{aligned} \tag{5}$$

When developing a suitable SVM strategy for the dual-inverter supply and considering (5), it seems logical to adapt the two-level SVM method for five-phase VSI of [16] accordingly. Considering that the two-level SVM method uses only large and medium active vectors during each switching period and these can now be applied from each side, there are nine possible vector combinations, as illustrated in Fig. 5. The nine vector combinations result in a total of 131 phase voltage space vector positions. Since there are 22×22 = 484 possible switching states then there are 353 redundant switching states. The space vector lengths and positions, in the *α-β* sub-space, generated by the vector combinations, are presented in Fig. 6 (zero-zero combination is omitted). The high level of redundancy, which exists, offers great scope for optimising the performance of the converter. The development of such algorithms is beyond the scope of this paper and is postponed for further work.

IV. Equal Reference Sharing Scheme

As shown in Fig. 7, the equal reference sharing scheme (ERS) uses two independent five-phase two-level space-vector modulators which utilise the SVM algorithm discussed in section II. The two-level modulators are operated in phase opposition as required by (5), that is to say both inverters

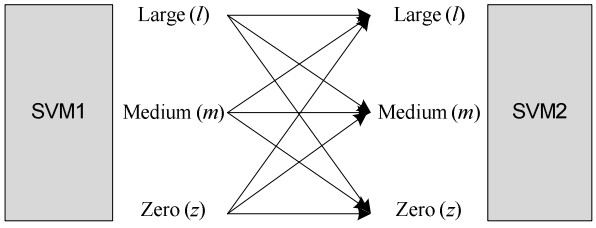

Fig. 5. Five-phase dual inverter switching combinations.

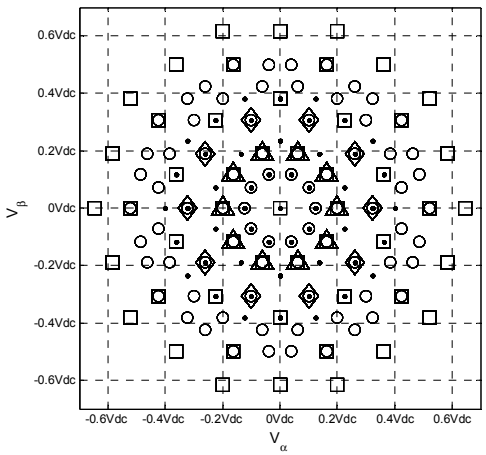

Fig. 6. Space vectors in α-β plane, created by *l-l* (□), *m-m* (●), *m-l, l-m* (○), *l-z, z-l* (◊), *m-z, z-m* (Δ) combinations.

operate in a complementary manner. In order to achieve this, the phase voltage reference is pre-multiplied by 0.5 and applied equally to each two-level modulator. This ensures that each inverter is supplying equal power to the machine. Furthermore, the voltage reference of inverter 2 modulator is shifted by 180 degrees in order to generate complementary switching of the two inverters: for instance, when the upper switch in leg A_1 (inverter 1) is on, the lower switch of leg A_2 (inverter 2) is on, and vice versa. The only other alteration required is the calculation of vector dwell-times (1)-(2), since dwell times are now governed by the dc link voltages of the individual inverters (V_{dc1} , V_{dc2}) and not the effective dc link (V_{dc}), which is the equivalent dc voltage of the single-sided supply mode.

Clearly, the ERS scheme has identical performance to that of the two-level topology in single-sided supply mode, since only 22 space vectors are utilised, leading to phase voltages with nine-level waveform. This has been verified via simulation and identical results to Fig. 3 were produced. Fig. 8 shows switching states of each inverter for M = 1.05 and confirms that they are operating in anti-phase. The short zero vector application time indicates that both inverters are operating in the linear region limit. Despite this scheme offering no advantage in terms of harmonic performance and number of levels, the topology has clear benefits regarding fault tolerant and EV applications.

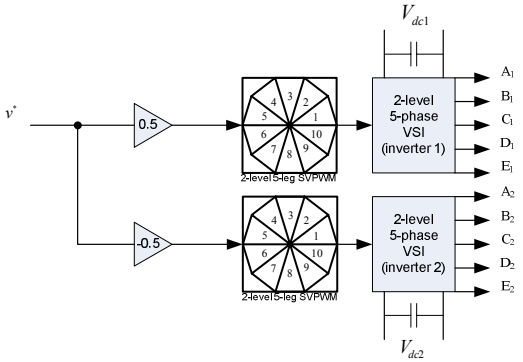

Fig. 7. Equal reference sharing scheme

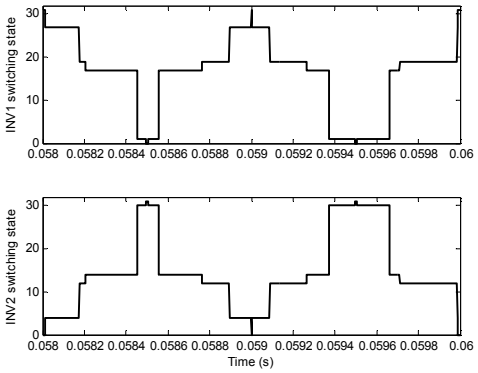

Fig. 8. Dual-inverter supply switching states for M = 1.05.

V. UNEQUAL REFERENCE SHARING SCHEME

The unequal reference scheme (URS), shown in Fig. 9, again uses two identical two-level modulators. However, the voltage reference applied to the modulators is apportioned according to the modulation index M. For clarity it is beneficial to define individual modulation indices as $M_1 = v_1^* / (0.5V_{dc1})$, $M_2 = v_2^* / (0.5V_{dc2})$. Inverter 1 only is operated up to the point when M = 0.525 (M_1 = 1.05). Hence the converter operates in two-level mode, since inverter 2 output is not modulated and the VSI switches between zero states 11111 and 00000. It is shown further on that the performance is significantly improved compared to the two-level and equal reference sharing schemes. When M > 0.525, inverter 1 is held at M_1 = 1.05 and inverter 2 output is modulated as well. These constraints can be expressed as:

$$\begin{aligned} &0 \le M \le 0.525 \quad \begin{cases} M_1 = 2M \\ M_2 = 0 \end{cases} \\ &0.525 \le M \le 1.05 \quad \begin{cases} M_1 = 1.05 \\ M_2 = 2(M - 0.525) \end{cases} \end{aligned} \tag{6}$$

Unequally apportioning the voltage reference between the two modulators leads to a greater number of switching possibilities than in the ERS scheme. The URS method will therefore result in multilevel operation and improved harmonic performance.

In order to verify and analyse the behaviour of the developed modulation methods, a number of simulations are performed for values of modulation index spanning M = 0.05 to M = 1.05 (0.025 increments). For the comparison purposes

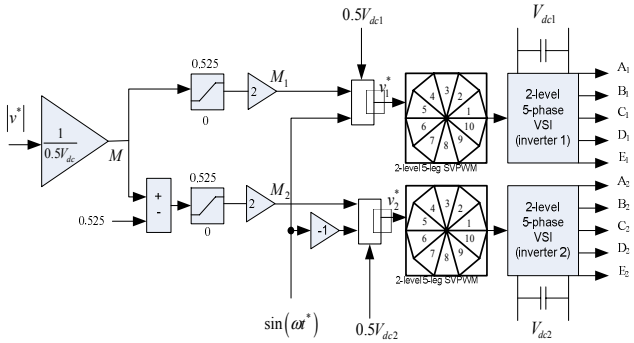

Fig. 9. Unequal reference sharing scheme.

both dual-inverter SVM methods are simulated. The dc link voltage of each inverter is set to 300 V (600 V single-sided supply mode equivalent), reference frequency is 50 Hz and the switching frequency of each VSI is 1 kHz. Selected simulation results are shown in Fig. 10 for M = 0.1, 0.6 and 0.9. The waveforms clearly show a change in the number of phase voltage levels (9, 15 and 17 for M = 0.1, 0.6 and 0.9, respectively). The spectra indicate that the low-order harmonic content is the lowest possible and the target fundamental voltages have been met. The 50% reduction in the effective dc link voltage is evident for M = 0.1, since only one VSI is utilised. The switching states of the inveters show that the modulation of inverter 1 is locked at M_1 = 1.05 when M > 0.525, while the other inverter output is modulated independently, according to the modulation index M_2.

The total harmonic distortion (THD) of the phase voltage is used as a performance indicator. It is calculated for each increment of modulation index according to:

$$THD = \sqrt{\frac{\sum_{n=1,2,3\ldots}^{r} v_n^2 - v_1^2}{v_1^2}} \qquad (7)$$

where v_n is the rms value of the n-th harmonics component, v_1 is the rms of the fundamental, n is the order of the harmonics used for calculation and r = 2000. A comparison of the THDs for the two SVM methods is presented in Fig. 11 and summarised in Table I. As expected, the number of phase voltage levels increases when M > 0.525. When $M \leq 0.525$, the URS scheme has a significantly improved THD, despite the phase voltage comprising only nine levels. In fact the THD is indentical to that of the ERS scheme when it is operating at twice the modulation index. This improvement in THD is entirely a consequence of the effective dc voltage, which is switched across the load. The URS method switches half of the dc voltage, while the ERS method switches full dc voltage. When M > 0.525, the second inverter output is modulated and the converter operates in multilevel mode up to M = 1.05. As a result of the multilevel output phase voltage, the THD is improved, compared to the ERS scheme.

Fig. 11 shows that the URS scheme has superior performance in both sub-spaces. The x-y sub-space is of particular significance since the impedance of the machine in this sub-space is very low. Thus any improvement in voltage

TABLE I. PERFORMANCE COMPARISON OF ERS AND URS SCHEMES.

	ERS	URS	
M	THD	levels	THD
0.05	5.2875	9	3.7504
0.1	3.7504	9	2.5788
0.2	2.5788	9	1.6992
0.3	2.0420	9	1.2625
0.4	1.6992	9	0.9738
0.5	1.4531	9	0.7483
0.6	1.2625	15	0.7574
0.7	1.1069	17	0.7831
0.8	0.9738	17	0.7737
0.9	0.8570	17	0.7496
1	0.7483	17	0.7176
1.05	0.6974	9	0.6974

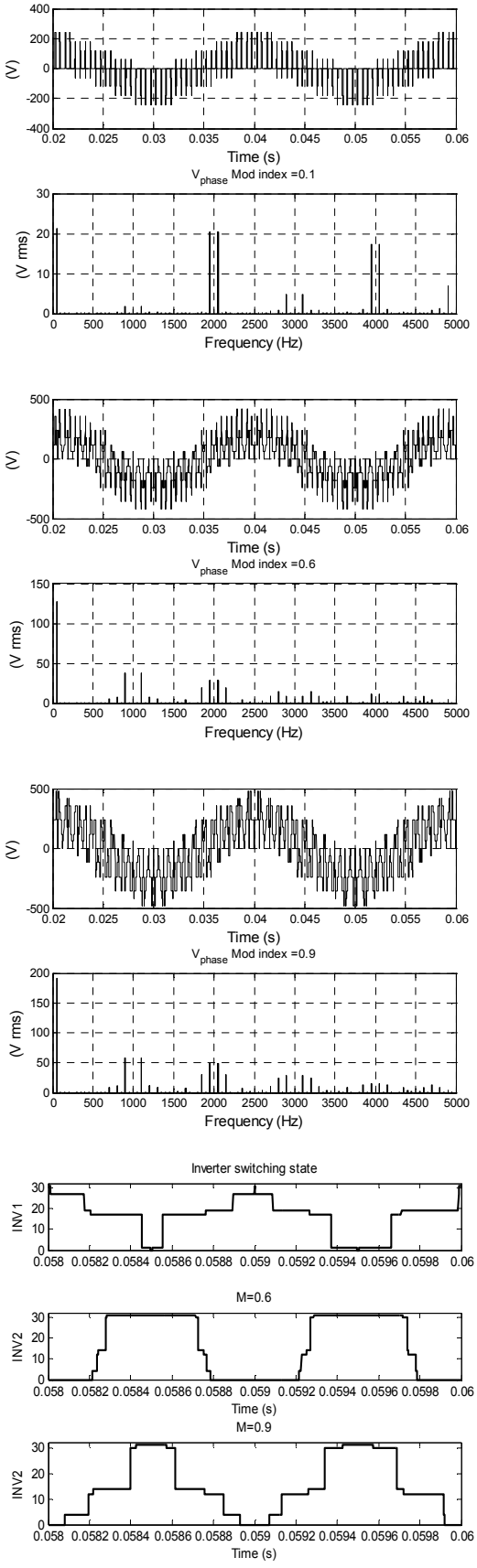

Fig. 10. URS scheme: phase voltage waveforms and spectra for M = 0.1, 0.6, 0.9 and the associated inverter switching states.

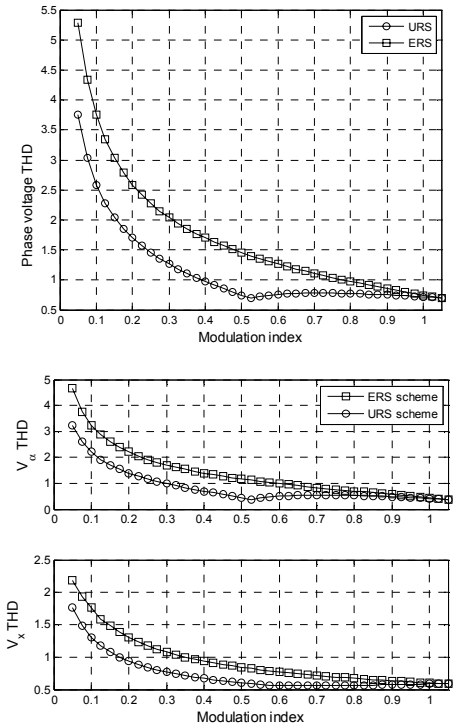

Fig. 11. Phase voltage, α-axis and x-axis THDs against modulation index for the ERS and URS SVM schemes.

THD will result in a marked reduction in machine losses. Fig. 11 and Table I show that the THD of the URS scheme ramains reasonably constant from $M = 0.6$ to 0.9, while there is a steady inprovement in the ERS case. It follows that the THD converges as the modulation index increases beyond 0.525. Finally, around the limit of the linear PWM ($M = 1.05$), the converter reverts to two-level operation.

Fig. 12 indentifies the voltage vectors in the α-β and x-y sub-spaces, which are triggered by the URS scheme for M values of $M = 0.6$ and 0.9. It can be seen that there are some differences in the space vectors used, which depend on the value of the modulation index. This leads to the phase voltage levels being a function of the modulation index.

VI. Conclusion

This paper has presented two SVM schemes for the dual-inverter five-phase open-end winding topology. The ERS scheme utilizes two standard five-phase two-level SVM modulators, one for each inverter, and switches the inverters in phase opposition. The URS scheme apportions the voltage reference to each modulator so that when $M \leq 0.525$ only one inverter output is modulated. When $M > 0.525$ both inverter outputs are modulated, with inverter 1 held at its maximum modulation index ($M_1 = 1.05$). The performance of the developed SVM methods has been verified by simulation and THDs have been evaluated. The results show that the ERS scheme performance is identical to a single two-level VSI. The URS scheme produces considerable improvement in the output phase voltage quality, as indicated by the lower value of THD for all values of the reference voltage, except when M reaches 1.05 and the converter reverts to two-level mode.

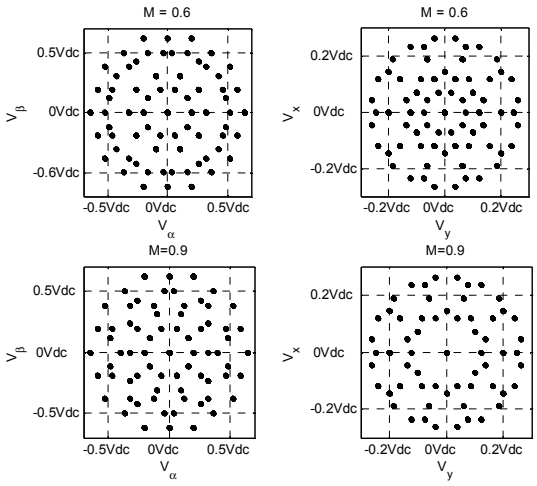

Fig. 12. Dual-inverter α-β and x-y voltage vectors for M= 0.6 and 0.9.

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