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A Wideband Gain Linearized Microwave Voltage Controlled Oscillator with Low Phase Noise Variation in Nanometer CMOS Technology*

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A wideband CMOS LC tank voltage-controlled oscillator (VCO) with low phase noise variations and a linearized gain has been designed using a new binary-weighted switched-capacitor and digitally-controlled varactor bank. The novel design has the advantages of more linear VCO frequency tuning, lower phase noise and reduced gain to variations in supply voltage. The proposed VCO has been designed using UMC 90-nm, 6-metal CMOS technology and features phase noise variation of less than 4.9 dBc/Hz. The VCO operates from 3.45 to 6.55 GHz, with phase noise of −133.4 dBc/Hz at a 1 MHz offset, a figure of merit (FoM) of −203.3 dBc/Hz, less than 41 dBm spurious harmonics, and a total VCO core current consumption of 1.18 mA from a 3.3 V voltage supply. To the authors' knowledge, this is the lowest phase noise variation ever reported.

Keywords: CMOS; MOMDCSA; phase noise variation; VCO gain; tuning range; figure of merit.

1. Introduction

Voltage-controlled oscillators (VCOs) are very important components in frequency synthesizers for wireless applications. The architecture of a conventional PLL frequency synthesizer, based on an LC-VCO phase-locked loop (PLL), is preferred because it exhibits low phase noise variation across the entire bandwidth. The design of VCOs is challenging, due to the characteristics of available varactors. Standard

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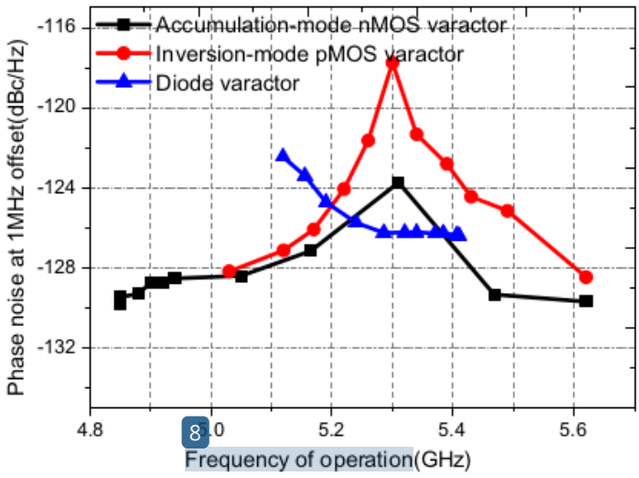

Fig. 1. Schematic diagram of the nMOS varactor and MOMDCSA circuit of the proposed CMOS VCO.

CMOS technology offers MOS capacitors and diodes as varactors. Inversion-mode pMOS varactors[1,2] and accumulation-mode nMOS can provide a significant VCO tuning range, but quality factor (Q) variation near the threshold causes VCO phase noise to fluctuate dramatically with the tuning voltage as shown in Fig. 1. In some designs phase noise variations exceed 20 dB[3] which is unusual. According to the information available to the authors, it seems that this problem is not as widely acknowledged in literature as it should be.

VCO gain (K_{VCO}) variation issues must be considered carefully when the tuning range of a VCO becomes very wide.[4] K_{VCO} variation increases in line with the frequency tuning range of the VCO, which creates an obstruction to optimizing the performance of the PLL.[3] In addition, using a MOS transistor as a varactor will increase the probability of converting AM noise to FM noise. Therefore, switching capacitors are mandatory for maintaining minimum phase noise, tuning linearity, and low VCO sensitivity when the tuning range is more than 30%.[3] Studies using switching capacitors inside the LC tank have been conducted, in order to extend the tuning range and improve VCO phase noise.[5–7] These techniques are effective in widening frequency tuning, improving phase noise performance and lowering K_{VCO}. However, the measured phase noise has been relatively high, varying from -90.2 dBc/Hz[5] to -122 dBc/Hz.[7]

In this work, we introduce a novel approach to gain linearization, in order to provide a significant improvement in VCO phase-noise performance. We implement this approach using a digitally switched varactor bank (DSVB) together with a new 4-bit metal-oxide-metal (MOM) digital capacitor switching array (MOMDCSA), which delivers reduced VCO tuning gain with low phase noise variation. Using this novel approach, we are able to optimize the VCO for phase noise and extend and linearize the tuning range. In order to reduce VCO phase noise variation, a varactor

bank is used and each pair in the bank is biased differently, to extend the range. Thus, the VCO tuning gain reduces and optimal phase noise is obtained across a wide range of frequencies, with minimum phase noise. When compared to recently reported work, the proposed VCO's bandwidth is increased by more than 10%, phase noise reduction by more than 10 dBc/Hz, and phase noise variation is measured at less than 4.9 dBc/Hz.

This paper is organized as follows: Section 2 introduces the VCO's core design and the implementation process, while Sec. 3 illustrates the concept of the digitally switchable MOM capacitor. Simulation and experimental results are presented in Sec. 4, and finally, conclusions are drawn in Sec. 5.

2. Circuit Design and Implementation

A fully integrated complementary cross-coupled VCO, based on a MOMDCSA, nMOS varactor pairs and DSVB, is depicted in Fig. 2. This configuration is chosen in this work because the structure offers higher transconductance, better rise- and fall-time symmetry and the active devices serve as a negative resistor to compensate for the energy loss from the tank due to the tank effective resistor. Another advantage of this topology is its ability to achieve low phase noise compared to other

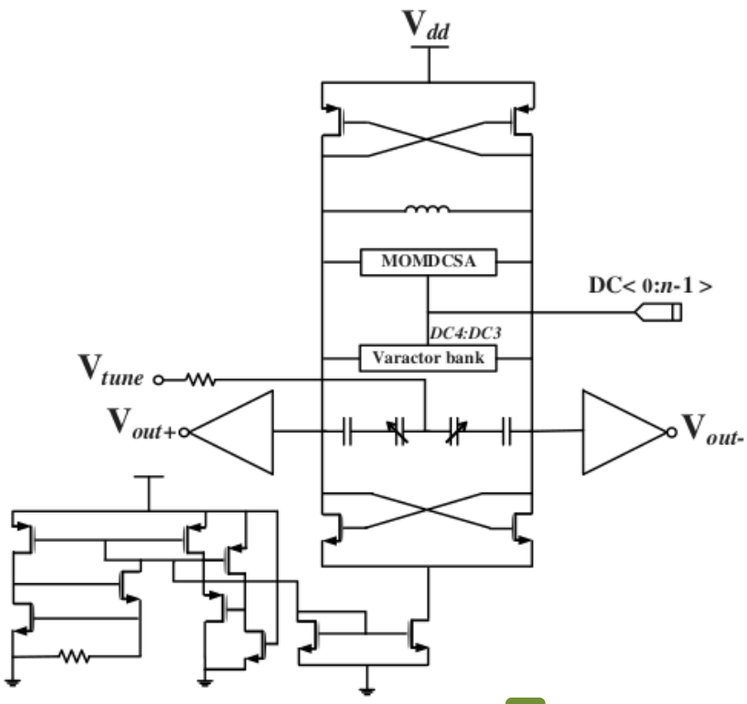

Fig. 2. Schematic diagram of the nMOS DSVB and MOMDCSA circuit of the proposed complementary cross-coupled VCO.

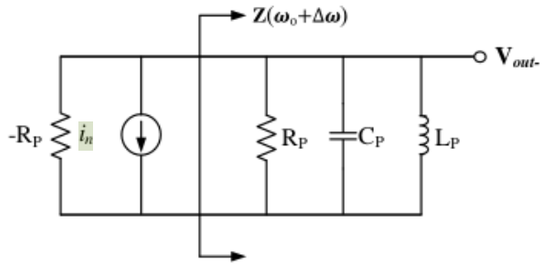

Fig. 3. Small signal equivalent circuit of the VCO.[4]

configurations.[8,9] The VCO is mainly composed of a single integrated differential spiral inductor, a varactor bank and a high-quality digital switching array to obtain linear tuning curves, minimum K_{VCO} and minor phase noise variations.

The phase noise can be analysed using Lee and Hajimiri's[10] model. LC-tank VCOs can be viewed as a parallel combination of a lossy LC tank with a negative resistance[8] as shown in Fig. 3.

The negative resistance must compensate for the losses of the LC tank parallel resistance, RP. The impedance of an LC-VCO tank may be approximated as:

$$Z(\omega_0 + \omega_0) \approx j \cdot \frac{R_P \omega_0}{2Q\Delta\omega}, \tag{1}$$

where Q is the quality factor of the LC-tank. The relationship between the phase noise and gain K_{VCO} at the output of the VCO can be shown as[11]:

$$S_{\phi n} = \left(\frac{K_{\mathrm{VCO}}}{S}|Z(\omega_0 + \Delta_0)|\right)^2 \cdot {i_n}^2 \alpha \frac{1}{Q^2}\left(\frac{K_{\mathrm{VCO}}}{2\Delta\omega}\right)^2. \tag{2}$$

Equation (2) shows clearly that the phase noise of the VCO is proportional to the square of the VCO gain. As discussed above, in order to obtain better phase noise with minimal variation, both VCO tuning gain and an extended linear tuning range are necessary.

3. Concept of Phase Noise Minimized Techniques

A wide tuning range is achieved by switching capacitors in popular wideband VCOs, in which the switched capacitors can be fixed capacitors or varactors. However, this leads to K_{VCO} and phase noise varying greatly over different sub-bands. Switched capacitors have worse phase noise due to their lower quality factor than fixed capacitors and noise from MOS switches being modulated directly to phase noise. Hence, switched capacitor arrays with MOM capacitors are implemented in this work for their low phase noise. A wide tuning range with low phase noise variation is achieved by combining the MOMDCSA, the nMOS varactor pairs and the DSVB, in

order to compensate K_{VCO} and overcome the problem of K_{VCO} variations over different sub-bands for minor phase noise variation.

The schematic of the proposed VCO is shown in Fig. 4, where the MOMDCSA is connected in parallel with the nMOS varator pair and the DSVB is implemented, to divide the tuning range into multiple frequency bands. Equal step sizes for the MOM capacitor values $(C_{\mathrm{MOM}}, 2C_{\mathrm{MOM}}, 4C_{\mathrm{MOM}}, \ldots, 2^{N-1}C_{\mathrm{MOM}})$ and nMOS device switch widths $(W_N, 2W_N, 4W_N, \ldots, 2^{N-1}W_N)$ are used to provide binary-weighted switching steps.

The MOMDCSA capacitance value can be calculated as:

$$c_{Sw} = (2^n - 1)\left(\frac{1}{C_{\mathrm{MOM}}} + \frac{1}{C_{\mathrm{df}}}\right)^{-1} + C_{\mathrm{par}}, \tag{3}$$

where C_{MOM} is the capacitance of the MOMDCSA, C_{df} is the drain fringe capacitances value of the switch devices, C_{par} is the fixed parasitic capacitances of the

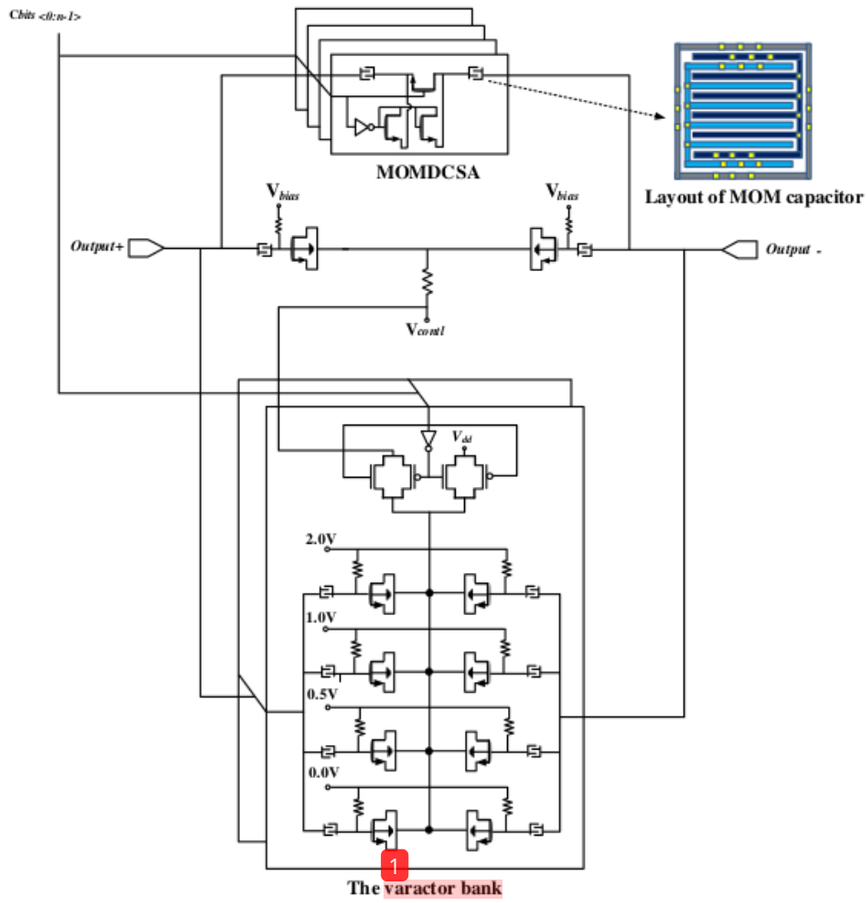

Fig. 4. Proposed tuning circuit, including MOMDCSA with nMOS DSVB and its logic control.

active devices. The total capacitances of the nMOS varactor pairs and the DSVB, C_{VB} is:

$$c_{\mathrm{VB}} = (2^n - 1)\left(\frac{1}{C_{\mathrm{MOM}}} + \frac{1}{C_{\mathrm{var}}}\right)^{-1}, \tag{4}$$

where C_{var} is the capacitances of the body-grounded nMOS varactor pairs and the DSVB when the group is selected to work as a conventional varactor. The oscillation frequency (f_{osc}) of the VCO can be written as follows:

$$f_{\mathrm{Osc}} = \frac{1}{2\pi\sqrt{L(c_{\mathrm{Sw}} + C_{\mathrm{VB}})}}. \tag{5}$$

K_{VCO} can be derived as:

$$|K_{\mathrm{VCO}}| = \frac{\partial f_{\mathrm{Osc}}}{\partial V_{\mathrm{cont}}} = \frac{(2^n - 1)}{4\pi\sqrt{L}} \cdot \left(\frac{C^2{}_{\mathrm{MOM}}}{\sqrt{C_{\mathrm{var}} + C_{\mathrm{MOM}}}}\right) \cdot \left[\frac{1}{C_{Sw} + (2^n - 1)C_{\mathrm{var}} \cdot C_{\mathrm{MOM}}}\right]^{3/2} \cdot \frac{\partial C_{\mathrm{var}}}{\partial V_{\mathrm{cont}}}. \tag{6}$$

Equation (6) demonstrates that the gain of the proposed LC-VCO is a function of the LC tank. It is easy to conclude that the gain decreases with the switching capacitor arrays. If the tuning range increases the phase noise variation will be significant and a large K_{VCO} variation will result. As such, there is an obvious trade-off between the required wideband frequency tuning range, phase noise variation and K_{VCO}.

To shift the tuning curves of the varactors, the four nMOS varactor pairs are biased at different voltages: 0, 0.5, 1 and 2 V. Such an arrangement will extend the linear tuning range of the varactor group, even though the linear tuning range of nMOS is minor. The control signal for each group in the varactor bank should be correlated to the control signal for the binary weighted switched-capacitor bank. When the varactor group is selected, it will operate as a conventional varactor tuned by change pump output; otherwise, it will serve as a fixed capacitor clamped by a fixed voltage.

To optimize VCO gain variation across the entire operating range, the 16 MOMDCSA sub-bands are divided into four subgroups, each of which corresponds to an operating mode of the proposed varactor bank. For example, the sub-group which covers the sub-bands between 7 and 4 will correspond to operating mode 01. A detailed configuration of digitally controlled varactor banks to all sub-bands is listed in Table 1.

The total linear tuning range is extended considerably, due to the overlapping linear tuning range among the four varactor pairs, while K_{VCO} and the phase noise have decreased considerably. In addition, phase noise variation is minimized in the proposed VCO using the novel MOMDCSA and nMOS DSVB. Each pair sets of the proposed varactor bank increases exponentially. Using both of the VCO tuning gain

Table 1. Working model of the varactor.

Group	Binary mode DC(4:3)	Sub-bands
1	00	0–3
2	01	4–7
3	10	8–11
4	11	12–15

linearized techniques above, K_{VCO} remains constant and is further reduced. It was found that this topology provides a relatively constant output swing and reduces K_{VCO} variation in line with the frequencies and minimizes phase noise over the operating frequency range. Consequently, the frequency tuning range, phase noise variation and K_{VCO} tradeoff is optimized.

4. Integrated Spiral Inductor

Generally, the key parameter for a fully integrated VCO performance in radio frequency integrated circuits (RFICs) is the quality factor of the on-chip inductors, capacitors, and varactors. The phase noise of an LC-VCO depends on the quality (Q) factor of the LC tank circuit: the higher the Q factor of the tank, the lower the phase noise.[3] The loaded Q factor of the resonator tank is primarily determined by the Q factor of on-chip inductors and varactors. The major drawback of on-chip inductors is the low Q factor and large die area. An approach has therefore been implemented and tested in this work to reduce the losses and obtain a high Q factor for on-chip inductors in CMOS technology.[12] This involves reducing the metal sheet resistance by using thicker metallization and lower resistivity metals. A single-layer centre-tapped symmetric inductor is implemented in 0.13 μm 1P8M RF CMOS process taken into consideration to obtain the maximum possible Q factor at the operating

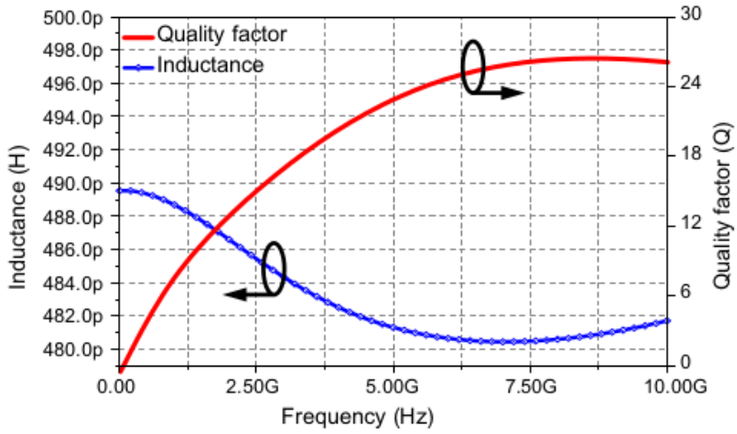

Fig. 5. Inductor values and quality factor of the centre-tapped differential inductor versus frequency.

bandwidth. The spiral inductor is designed to sit on the thick top metal layer to minimise ohmic loss and substrate parasitic capacitance.[13] The underpass part of the inductor is located on Metal-5, and the centre-tap on Metal-4. The thickness of the top metal is 1.2 μm and both Metal-5 and Metal-4 have a thickness of 0.43 μm. The Q factor and inductance were simulated at different frequencies, as shown in Fig. 5. The simulated Q factor for the designed inductors was 22.64 for 481.3 pH inductors, and the area was 16596 μm^2.

5. Simulation Results

The proposed VCO was implemented using a commercially available UMC-90 nm, 6-metal, mixed-mode CMOS process and simulated using Cadence Virtuoso Analogue Design Environment Tools. Figure 6 shows the layout of the proposed VCO, which occupies a silicon area of 1020×792 μm^2, not including the bond pad.

The simulated phase noise result at 1 MHz offset from the carrier frequency was -133.4 dBc/Hz, with variation between -136.20 dBc/Hz and -132.3 dBc/Hz, within the novel technique sub-tuning band, whilst the control voltage was kept constant. It is difficult to provide reasonably fair comparisons amongst different VCOs, but it is important to verify the efficiency of the new design. For this reason, a VCO was designed using binary-weighted switched capacitor (BWSC) VCO with one nMOS varactor pair to compare the performance with the novel VCO. Phase noise variation and the VCO gain of both VCOs were simulated as a function of the

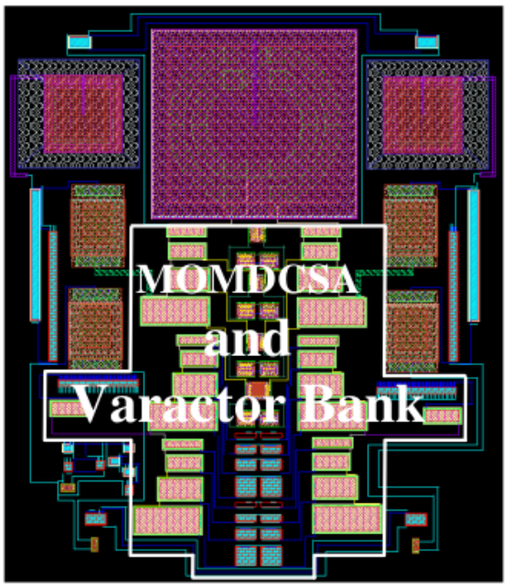

Fig. 6. Layout of the designed CMOS VCO with MOMDCSA and nMOS DSVB.

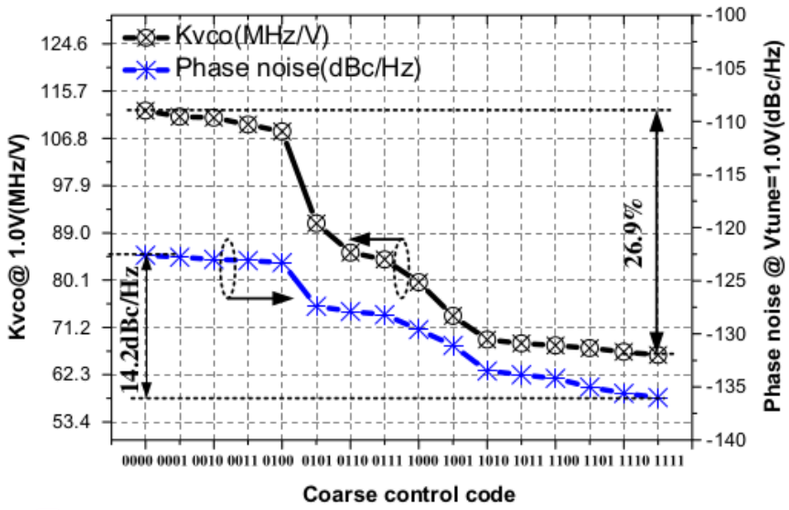

Fig. 7. VCO gain and phase noise of the proposed VCO using BWSC with one varactor pair as function of control codes.

control code of the switchable capacitor bank, while the analog varactor control voltage was fixed at 1.0 V. The results in Figs. 7 and 8 demonstrate that the phase noise variation is minimized from 13.6 to 4.8 dBc/Hz. All phase noise measurements were performed at a 1 MHz offset from the carrier. Furthermore, VCO gain variation is reduced from 26.6% to 4.6%. As a result, the new varactor achieves a steep transition for tuning voltages varying from 0 to 2.5 V.

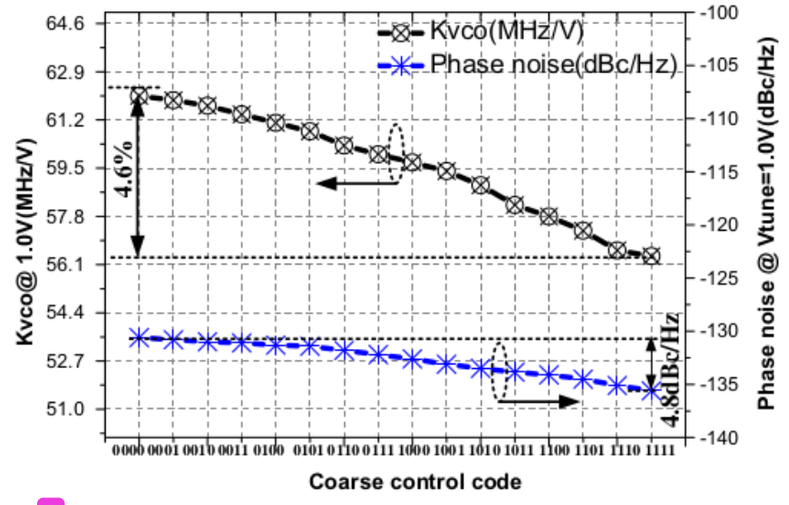

Fig. 8. VCO gain and phase noise of the proposed VCO using MOMDCSA, *n*MOS varactor pair and DSVB as function of control codes.

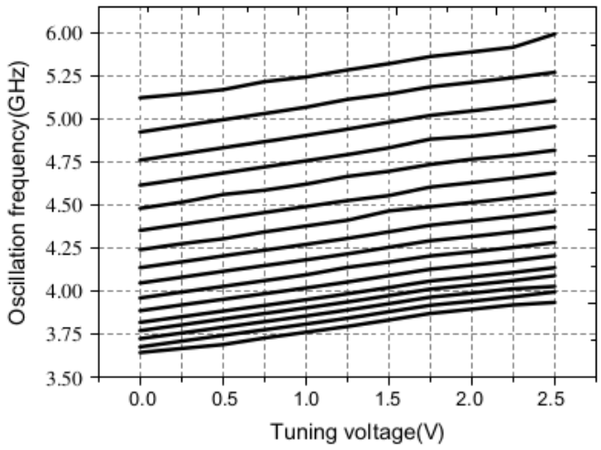

Fig. 9. Oscillation frequency characteristics versus tuning voltage of the proposed VCO using BWSC with one varactor pair.

The simulation results shown in Figs. 9 and 10, respectively, indicate that the proposed VCO exhibits a wider tuning range. The FoM model adopted by Ham and Hajimiri,[10] which normalizes measured phase noise with respect to center frequency and power consumption, is defined by Eq. (7):

$$\text{FOM} = L\{\Delta f\} - 20\log\left\{\frac{f_0}{\Delta f}\right\} + 10\log\left\{\frac{Pd}{1\,\text{mW}}\right\}. \tag{7}$$

The simulated FoM of the proposed VCO varies from $-201.8\,\text{dBc/Hz}$ to $-204.1\,\text{dBc/Hz}$ and the tuning range is increased from 3.63–5.94 GHz to 3.45–6.55 GHz, as shown in Fig. 11, upon implementation of the novel varactor.

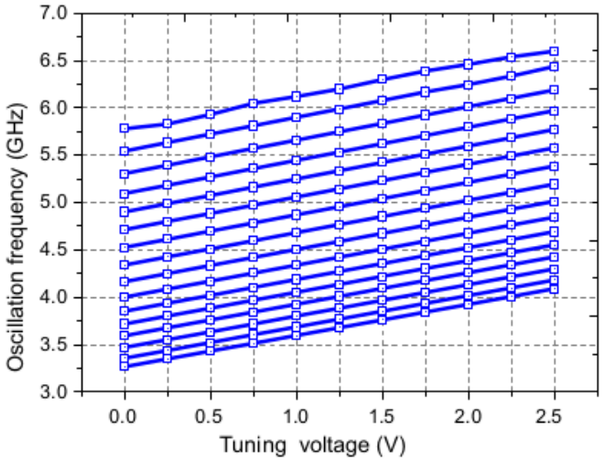

Fig. 10. Oscillation frequency characteristics versus tuning voltage of the proposed VCO using MOMDCSA, nMOS varactor pair and DSVB.

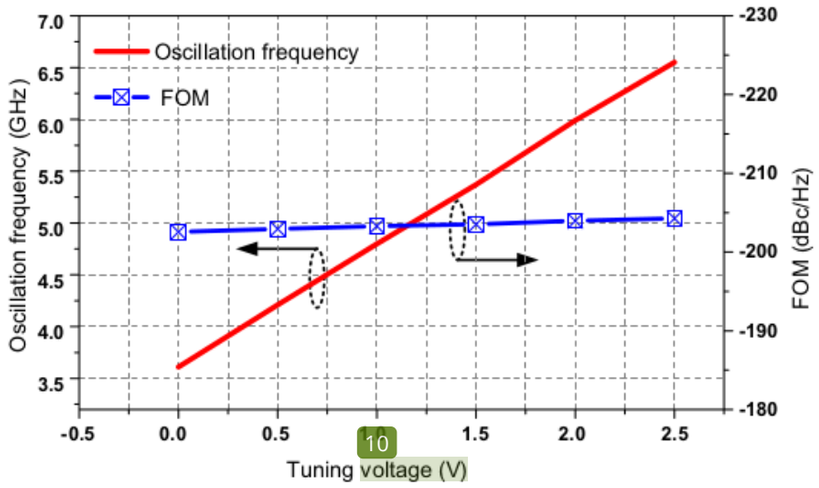

Fig. 11. Tuning characteristics and FoM of the proposed VCO using MOMDCSA, nMOS varactor pair and DSVB.

The phase noise of an LC-VCO is described, according to Leeson,[9] as:

$$L(f_m) = 10 \log \left[\frac{1}{2} \left(\left(\frac{f_0}{2Q_l f_m} \right)^2 + 1 \right) \left(\frac{f_c}{f_m} + 1 \right) \left(\frac{FKT}{P_s} \right) \right]. \tag{8}$$

As an illustration of the novel-varactor's usefulness, the single sideband (SSB) phase noise was simulated at 1 MHz offset from the carrier frequency was -133.4 dBc/Hz as

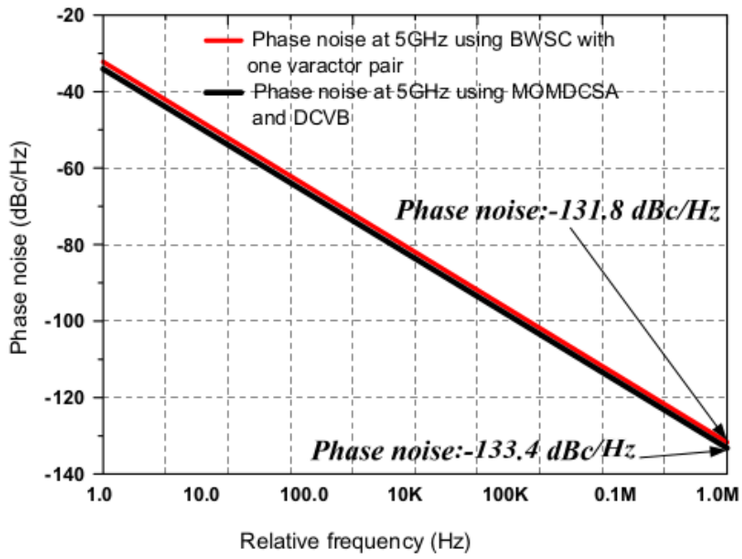

Fig. 12. Comparison of VCO phase noise using BWSC with one varactor pair and the proposed VCO with MOMDCSA, nMOS varactor pair and DSVB at 1 MHz offset.

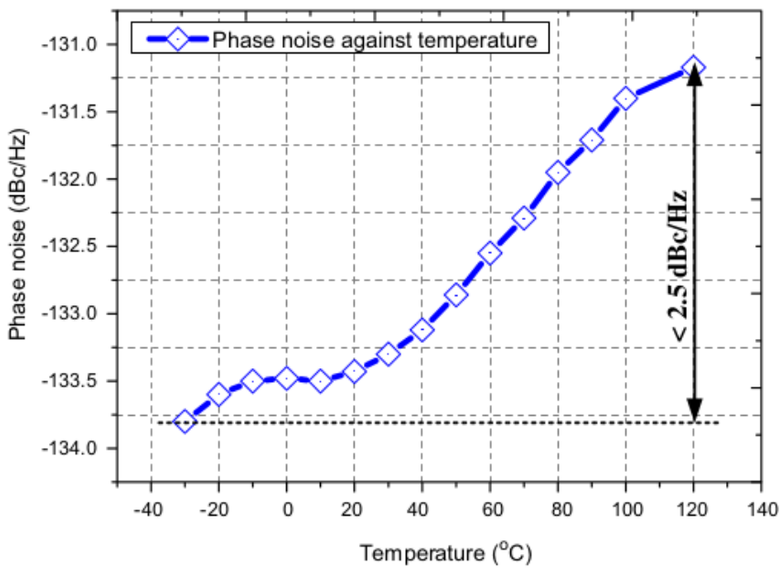

Fig. 13. Phase noise variation against temperature in degree Celsius (°C).

shown in Fig. 12. It can be observed that the phase noise is reduced by 1.6 dBc/Hz by the proposed VCO. Importantly, the proposed topology of the CMOS VCO achieves low phase noise with minimal variances through the bandwidth's sub-bands. The simulated phase noise variation versus temperature was < 2.5 dBc/Hz as shown in Fig. 13.

As can be seen, the new varactor design achieves steep transition with low K_{VCO} and minor phase noise variation. As proof of the concept, the performance of the novel VCO in this study is compared in Table 2 to other state-of-the-art designs in 0.09 μm, 0.13 μm and 0.18-μm CMOS technologies, the results showing clearly that the novel VCO is the best in terms of phase-noise, power dissipation, bandwidth and FoM, not only for fabricated work but also for simulated designs as well.

A comparison of the two state-of-the-art VCOs with the proposed VCO with MOMDCSA and DSVB is shown in Table 2. The proposed topology has better characteristics than the other VCOs with regard to power consumption and FoM,

Table 2. A comparison of the two state-of-the-art VCOs with the proposed VCO.

	Ref. 5	Ref. 7*	This work
Phase noise variances	—	4.06 dBc/Hz	~4.8 dBc/Hz
Phase noise at center frequency*	−90.2 dBc/Hz	−120.00 dBc/Hz	−133.4 dBc/Hz
FoM@1 MHz offset	−154.8 dBc/Hz	−185.6 dBc/Hz	−203.3 dBc/Hz
Tuning range	4.1–5.0 GHz	3.14–5.28 GHz	3.45–6.55 GHz
K_{VCO} variation	< 5%	—	~Γ4.6%
Power consumption (mW)	7.20 mW	5.40 mW	39 mW

*Simulated work.

Table 3. Performance comparison of CMOS VCOs.

Process (μm)	F (GHz)	P (mW)	PN (dBc/Hz)	Offset	TR (GHz)	FoM (dBc/Hz)	Ref.
0.18	5.00	7.20	−90.20	1.0	4.10–5.00	−154.80	5
0.18	4.20	4.50	−119.0	1.0	3.14–4.80	−184.47	7[S]
0.18	5.00	13.00	−121.5	1.0	5.10–5.36	−192.10	14[S]
0.18	5.20	9.70	−113.7	1.0	4.39–5.26	−180.00	15
0.18	5.80	10.08	−117.0	1.0	5.27–6.41	−184.00	16
0.18	5.10	9.70	−122.4	1.0	4.80–5.40	−189.60	17
0.18	6.98	3.40	−108.1	1.0	6.54–6.98	−180.00	18
0.09	3.95	6.60	−147.0	10.0*	3.40–4.50	−191.00	19
0.13	5.00	3.90	−133.4	1.0	3.45–6.54	−203.30	This work

Note: F: Center frequency, P: power, PN: phase noise at 1 MHz, *at 10 MHz offset TR: tuning range, FoM: figure of merit, S: simulation.

and it also has a more significant reduction of phase noise variations and improvement to the tuning range. Nonetheless, average K_{VCO} gain and gain variations can be reduced further by increasing the sub-bands to 16 with four-bit MOM switching.

6. Conclusion

Using a novel topology, a wideband LC-VCO has been designed and simulated using a UMC-90 nm mixed-mode CMOS process for high performance. An ideal VCO utilizing an MOMDCSA, an nMOS varactor pair and a DSVB has been implemented, with a broadband tuning range from 3.45 GHz to 6.55 GHz, approximately 62%, which varies linearly with the control voltage. We can conclude that the proposed MOMDCSA topology has better characterisation than other switches and a more significant effect on the reduction of phase noise variations. The high performance VCO specifications include measured phase noise of −133.4 dBc/Hz at an offset frequency of 1 MHz away from 5.0 GHz FoM of −203.3 dBc/Hz, while the VCO core's total power consumption is 3.9 mW using a 3.3 V supply voltage. The output peak-to-peak voltage of the VCO is 2.6 V, with excellent spurious harmonics at < 41 dBm. For CMOS, there are currently no published VCO designs featuring this topology, its performance or specifications. As proof of the concept, the performance of the novel VCO in this study is compared in Table 3 to other state-of-the-art designs in 0.09 μm, 0.13 μm and 0.18 μm CMOS technologies, the results showing clearly that the presented VCO is the best in terms of phase-noise, power dissipation, bandwidth and FoM, not only for fabricated work but also for simulated designs as well.

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